- Fully compliant with ARIB STD-B44.

- Automatic slot and frame acquisition using received header and TMCC signalling information.

- BPSK, QPSK, 8-PSK, 16-APSK and 32-APSK supported.

- Support for an arbitrary range of symbol rates up to 40% of the master clock frequency.

- Two-stage, stepped carrier search provides wide acquisition range.

- Integrated LDPC and TMCC decoding.

- Baseband I/Q radio interface incorporating compensation for DC offset and quadrature imbalances.

- Pilot-assisted carrier tracking ensures robust performance in the presence of high levels of phase noise.

- Physical layer sync acquisition and maintenance at −2dB SNR (Es/N0).

- Digital decimation and channel filters reject up to +10dBc of adjacent channel interference.

- Fully-digital carrier and clock recovery circuits eliminate the need for an external VCXO.

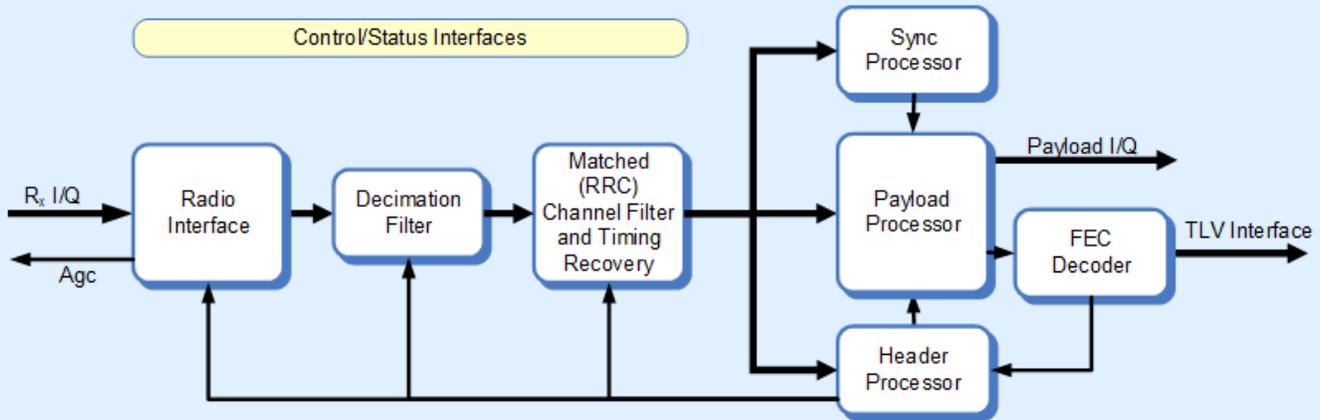- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).
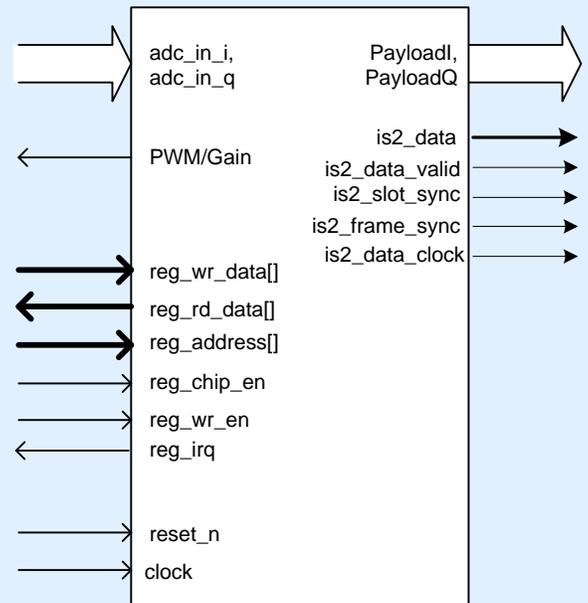
Contact information

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845

Block Diagram

Detailed Description

The Commsonic CMS0071 ISDB-S3 Demodulator is a high-performance (A)PSK demodulator core intended for ARIB STD-B44 ISDB-S3 advanced wide-band digital satellite standard.

Operating symbol rate is programmed from a register and extends from approximately 40% of the master clock frequency down to an arbitrary low rate that is set through synthesis options. The range would normally be dictated by the application and, in particular, the phase noise characteristics of the radio system.

Carrier acquisition is performed in several stages starting with a coarse, stepped search. The search range and step size are programmed through registers and can be set to accommodate an arbitrary offset (within the sample rate bandwidth).

Payload symbols are output as soft decisions after descrambling and the recovery of carrier phase, symbol timing and gain.

The CMS0071 is provided with a baseband I/Q radio interface compatible with zero-IF and near-zero-IF tuner modules. The interface performs automatic compensation of DC offsets and quadrature imbalances (phase and amplitude).

Tuner Rx gain control is provided through PDM output RxAGC. Further stages of gain control are implemented digitally within the demodulator.

The Decimation Filter stage suppresses wideband interference and restricts the sample rate bandwidth prior to matched (RRC) channel filtering and timing recovery. The combined response of the Decimation and Channel Filters allows the CMS0071 to tolerate up to +10dBc of adjacent channel interference at any supported symbol rate.

Three dedicated processors at the output of the Channel Filter handle the ISDB-S3 specific demodulation functions:

Sync Processor. This is responsible for the recovery of initial Physical Layer (PL) frame and slot synchronisation from the Start of Frame (SOF) sequences at the start of each slot.

Header Processor. This is responsible for configuring the Payload Processor according to the decoded TMCC signalling information which defines the slot configuration, modulation format and FEC code rate of the slots within the ISDB-S3 frame structure.

Payload Processor. This delivers soft output symbols (unsliced constellation samples) to the LDPC Decoder after carrier phase correction, gain normalisation and PL descrambling.

Detailed Description (Cont'd)

Register Configuration

Static configuration and status monitoring is performed through a bank of registers. This would typically be driven from a processor interface connected to a CPU that is embedded on the same device or located off-chip.

Parameters accessible through this interface include:

- Nominal symbol and input carrier frequencies;

- Window and step sizes for the coarse carrier search;

- AGC and PLL configuration and status;

- Estimated signal-to-noise ratio (CNIR).

Important synchronisation events such as the acquisition of symbol timing lock or PL frame sync are signalled through the SyncEvents output. Some or all of these signals would typically be connected to the processor interface as sources of interrupt but might otherwise be polled as status indicators.

The Channel and Decimation Filters use hard-wired FIR filter coefficients that are generated during synthesis. FPGA platforms employing more than one Channel Filter configuration would normally store a different netlist for each filter used.

The option of programmable coefficients is available for ASIC and high-end FPGA platforms that have adequate (multiplier) resources.

Full details of the register interface are provided in the CMS0071 IP Guide document.

Principle I/O Description

Register Bus Interface	
reg_address[]	Register address select input.
reg_chip_en	Block select input for the CMS0071 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data[]	32-bit Write data input.
reg_rd_data[]	32-bit Read data output.
reg_irq	Core Interrupt.

Radio Interface	
adc_in_i/q[9:0]	Complex receive samples at the core master clock frequency. Typically, 8-10bits depending upon the tuner filter specification and adjacent channel requirements.
PWM/Gain	Tuner receive gain control. Typically, a single-bit PDM signal but can be configured as a parallel output.

Demodulator Output Interface	
PayloadI/Q[9:0]	Payload Rx constellation sequence after carrier phase, symbol timing and gain correction.
SymbolStrobe	Qualifier for the samples delivered from PayloadI/Q output. The average rate is equivalent to the received symbol rate.

TLV Interface	
is3_data	8-bit ISDB-S3 TLV data output
is3_data_valid	is3_data data valid output.
is3_slot_sync	ISDB-S3 Slot start sync output.
is3_frame_sync	ISDB-S3 Frame start sync output.
is3_data_clock	ISDB-S3 data clock output.

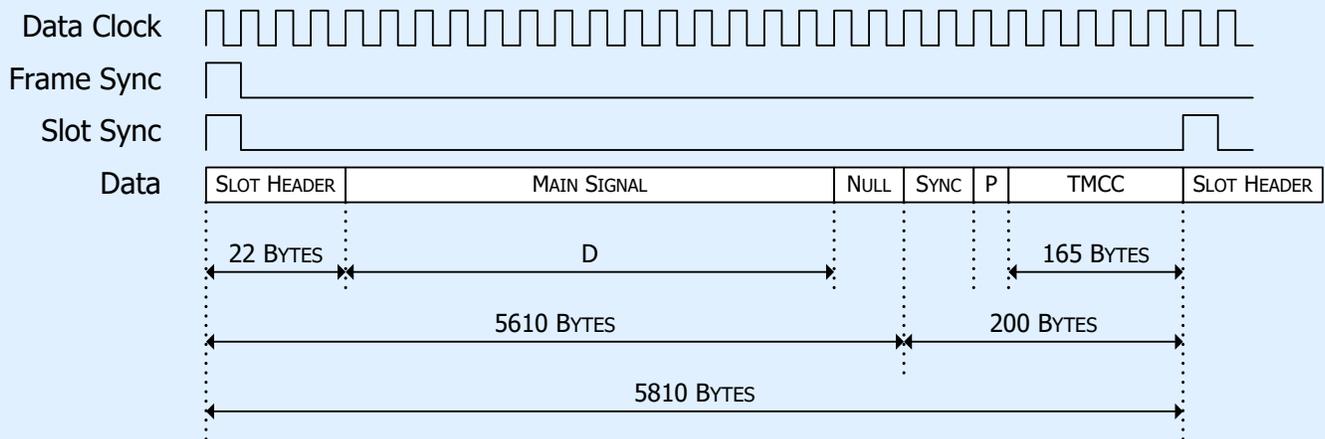| Others	
clock	Master clock input at a rate not less than 2.5x the maximum operational symbol rate.
reset_n	Asynchronous active-low reset input.

Timing Diagrams

Radio Interface:

clock

adc_in_i/q[9:0]

Sample latched
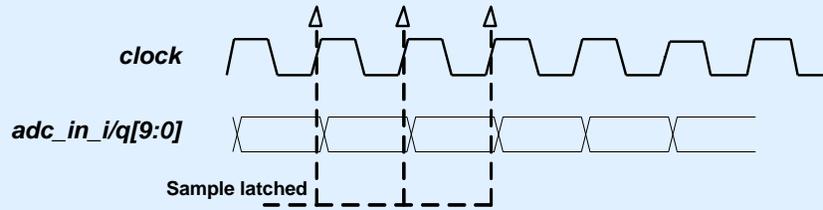
TLV Interface:

The standard interface supplied generates a TLV stream output at a rate linked to the recovered on-air symbol rate. The output stream provides all the information required to interpret the decoded ISDB-S3 frame.

Data Clock

Frame Sync

Slot Sync

Data | SLOT HEADER | MAIN SIGNAL | NULL | SYNC | P | TMCC | SLOT HEADER

22 BYTES

D

165 BYTES

5610 BYTES

200 BYTES

5810 BYTES

Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I²C, 8-bit, big-endian, little-en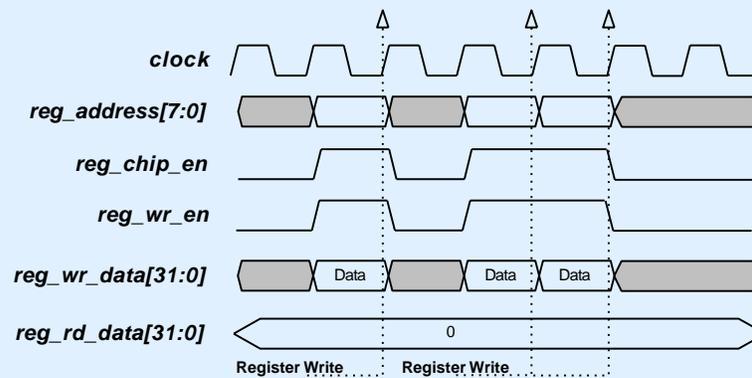dian, etc). The register-core can be interface directly with the Altera SOPC/QSYS builder via the Avalon bus using a zero wait-state configuration.

An active-high interrupt line is also available.

Register read access:
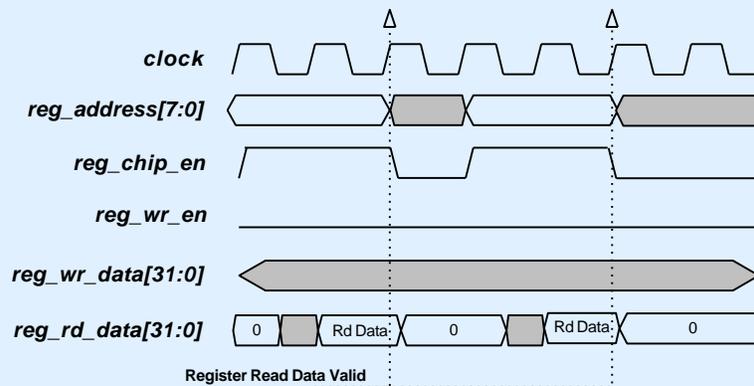
Register write access:

Altera® Megacore®

The ISDB-S3 Demodulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2/S2X, ISDB-S3, DVB-C/J.83/A/B/C, DVB-CID, ATSC 8-VSB, ISDB-T and DVB-T/H/T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.