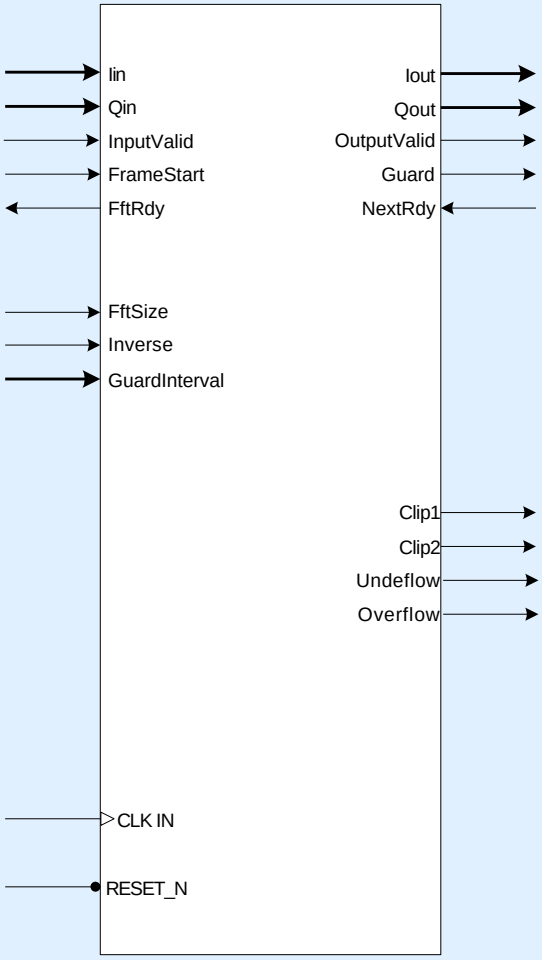
General-purpose FFT core

CMS0001

- Typical applications include COFDM modems for 802.11a, 802.16 and DVB-T.
- Synthesis controls allow FFT sizes = 2^n with support for multiple run-time sizes such as 2k/4k/8k modes for DVB-T/H.
- Performs forward or inverse FFT.
- Generates cyclic prefix as required by most COFDM standards.
- I/O structures support both Time Domain (real-time) and Frequency Domain (burst mode) interfaces.
- Synthesis control of signal precision (variable width).

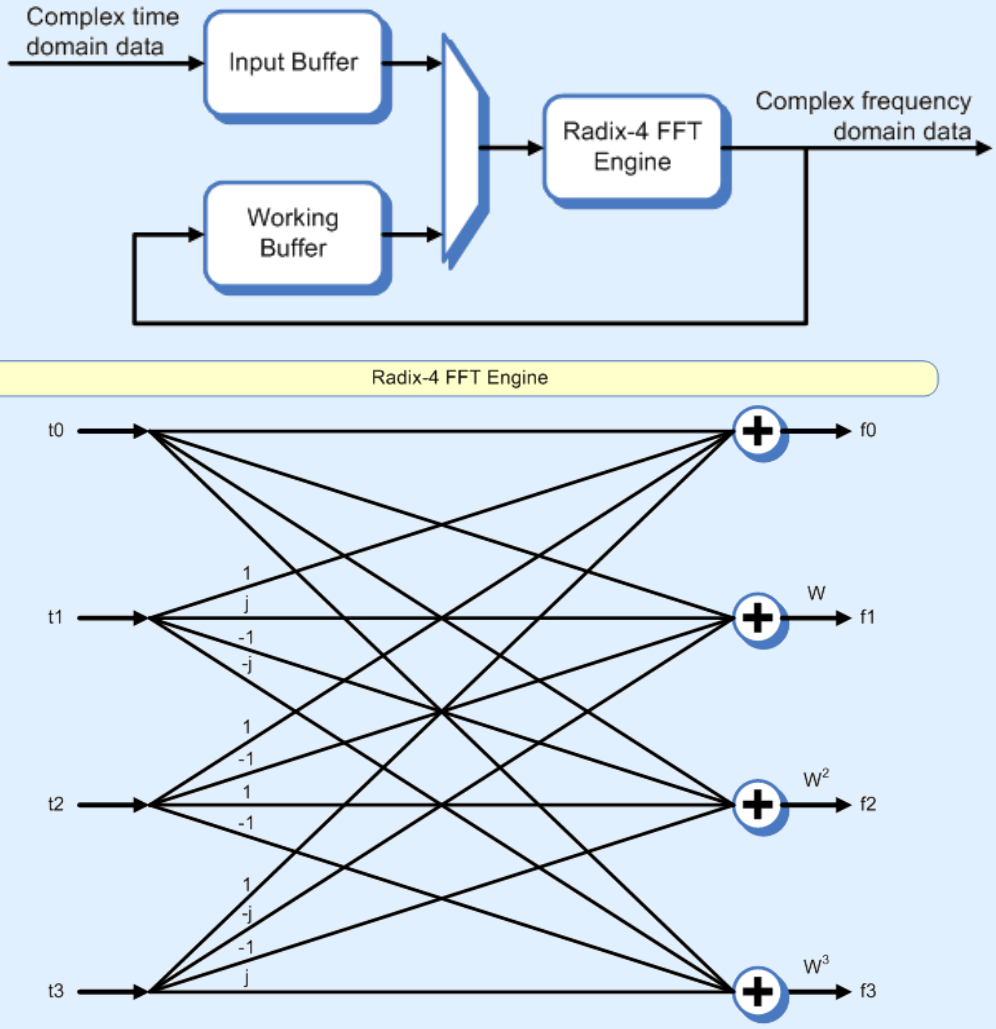


Contact information

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845

Block Diagram



Detailed Description

FFT Computation

The FFT is factored into Radix-4 Butterfly operations. When an odd power of two is required, a small radix-2 "follower" stage performs the final iteration. The radix-2 stage does not require a full complex rotator so its cost is minimal.

The Radix-4 Engine fetches one complex word of data each clock cycle. Four interleaved data words are collected then applied to the t0-t3 inputs. On successive clock cycles the engine calculates the four frequency domain outputs f0-f3. These are then stored back into the Working Buffer.

During the final iteration, the engine produces frequency domain outputs on successive clocks. These arrive in scrambled (digit-reversed) order.

A final pass through the data produces outputs in sorted order.

Detailed Description (Cont'd)

Ram Buffer Architecture

The FFT core may be synthesized with one two or three RAMs, depending on throughput and I/O timing requirements. Each RAM cycles through an input phase, a work phase and an output phase.

Typical applications use two RAMs: one for real-time I/O while the other is computing.

In a modulator, the frequency-domain (carrier) data bursts into the IFFT at clock rate, the time-domain values are calculated at clock rate, then the output of the IFFT is read out slowly, in real-time. During the output of the first IFFT frame, the next frame is being computed in the second RAM.

Similarly, demodulator (time-domain) inputs are gathered slowly in real time. Once a full FFT frame is acquired, the FFT is computed quickly and the frequency-domain outputs are read out in a burst. The second RAM acquires inputs while the first is used for computation and output.

A single RAM may adequately service some applications if 1) both input and output are bursted and 2) total processing time is within budget.

Timing Information

Processing delay from last input to first output = ***FFTsize * log4(FFTsize) + pipeline delay.*** For odd powers of two use next lower power of four when computing ***log4()***. For example, a 2048-point FFT requires five layers of radix-4 butterflies (***log4(1024)***) with an additional layer of radix-2 butterflies. The computation time is 2048 * 5 + pipeline delay (about 12 clocks).

Real-Time Mode Controls

The mode controls `fft_size`, `inverse` and `guard_interval` are not pipelined. Any data remaining in the FFT block when the mode changes may be corrupted. If the system requires re-use of the FFT in different modes, it must complete all processing of the current mode before the next mode is initiated.

Principle I/O Description

Input Port	
i_in	Real part of complex input data
q_in	Imaginary part of complex input data
input_valid	Indicates clock cycle on which data inputs are valid
frame_start	Indicates current input sample is the first sample of the FFT frame. Must occur with input_valid = 1.
fft_rdy	Indicates the FFT can accept another input value. Data is transferred on cycles when input_valid = fft_rdy = 1.
Output Port	
i_out, q_out	Complex outputs
output_valid	Indicates output I/Q are valid
guard	Indicates first sample of cyclic prefix, or if none then the start of the FFT output frame
next_rdy	Indicates the next block can accept FFT output data Data is transferred on cycles when output_valid = next_rdy = 1.
Mode Control	
fft_size	Current FFT size. Must be a power of two. This is typically decoded from a mode control register.
inverse	0 => forward FFT 1 => inverse FFT
guard_interval	Number of samples of cyclic prefix generation. May be set to zero
Status Outputs	
overflow	input_valid = 1, but fft_rdy = 0 (not ready for input) This signal is typically true in modulators, but can indicate flow problems in a demodulator.
underflow	next_rdy = 1, but output_valid = 0 (output data not available) This signal is typically true in demodulators, but can indicate flow problems in a modulator.
clip1_event	Normally low, this output pulses high if the radix4 engine clips
clip2_event	Normally low, this output pulses high if the output stage clips

Synthesis Controls

supported_sizes	Supported FFT sizes must be powers of two. Set the corresponding bit in this word for each size supported.
input_width	Bit-width of input I and Q
input_fract_bits	Number of fraction bits for I and Q inputs
work_width	Bit-width of working RAM I and Q. This typically includes two bits of headroom above the input width and might also include 1-2 fraction bits.
work_fract_bits	Number of fraction bits for the working RAM. This is used to align the input data within the working data word.
extra_fract_bits	Number of extra fraction bits retained from the real partial multiplies when calculating complex rotations. These extra bits are subsequently rounded from the complex results.
output_width	Bit-width of output I and Q
output_fract_bits	Number of fraction bits for the output I and Q values. Output values are clipped and rounded from the working width
twiddle_width	Bit-width of the sine-cosine table. Includes a sign bit, with the rest fractions. Sine-cosine values range from 100…01 to 011…11
build_odd_gain_correction	If this is enabled, the radix2 engine incorporates a root-2 gain correction factor. Useful in a modulator to keep power level constant in different modes. In a demod, the FFT is usually inside a gain-correcting loop so does not require this correction.
split_inputs	Inverts the MSB of the input address. In an IFFT, this shifts the zero frequency to the center of the band.
split_outputs	Inverts the MSB of the output address. In an FFT, this shifts the zero frequency to the center of the band.
sincos_decimation	Typically 1 (not decimated). However, in some applications it is possible to decimate the sine-cosine tables by a factor of 2x or 4x without compromising performance. Sine-cosine tables are generated at the resolution of the largest supported fft_size / sincos_decimation.
supported_sizes	Supported FFT sizes must be powers of two. Set the corresponding bit in this word for each size supported.
input_width	Bit-width of input I and Q
input_fract_bits	Number of fraction bits for I and Q inputs
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work_fract_bits	Number of fraction bits for the working RAM. This is used to align the input data within the working data word.

About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S2, DVB-C/J.83/A/B/C and DVB-T/H.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845