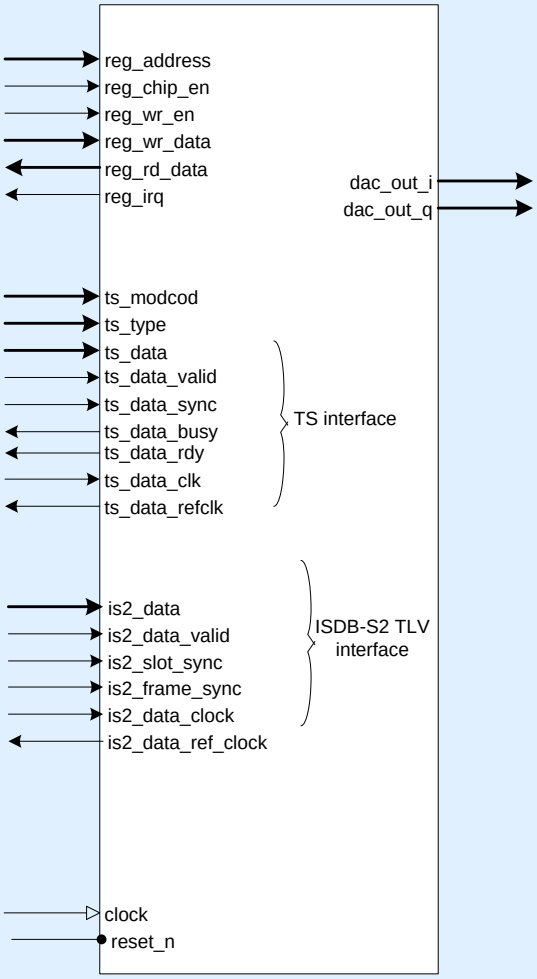
ISDB-S3 Modulator

CMS0070

- Fully compliant with ARIB STD-B44.
- Variable sample-rate interpolation provides ultra-flexible clocking strategy
- BPSK, QPSK, 8-PSK, 16-APSK and 32-APSK supported.
- Integrated LDPC channel coder.
- Integrated TMCC channel coder.
- Optional simultaneous DVB-CID modulation.
- Automatic frame construction from input TLV stream.
- Optional internal IF conversion.
- Optional noise interference source.
- AD9857/AD9957 interface and auto-programming support.
- Modes that are not required may be removed with synthesis options to generate a compact, efficient design.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



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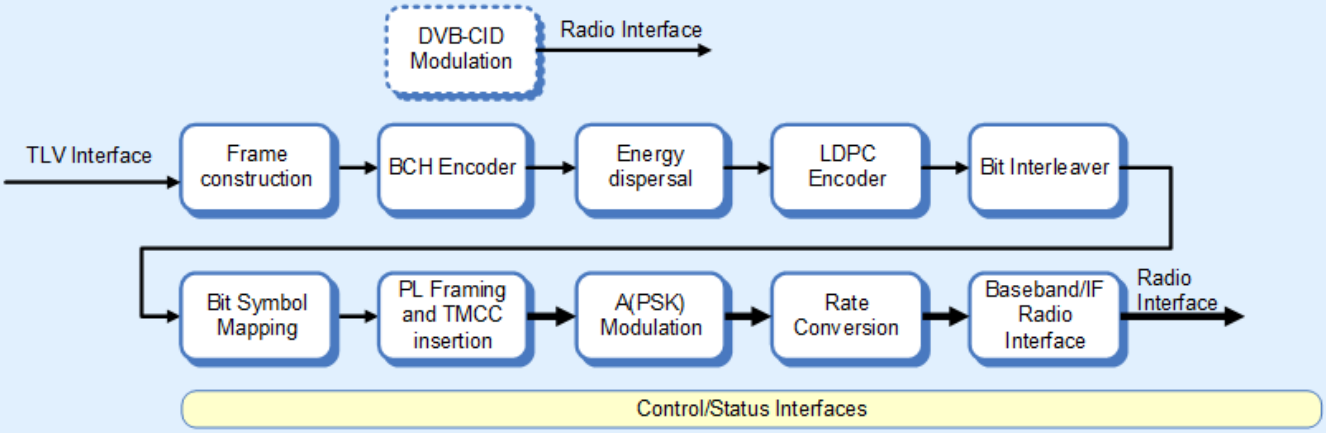
Block Diagram



Detailed Description

The Commsonic CMS0070 ISDB-S3 Modulator with integrated LDPC encoder has been designed specifically to address the requirements of the ARIB STD-B44 advanced wide-band digital satellite standard.

The core provides all the necessary processing steps to modulate a single transport stream (or baseband-frame) into a complex I/Q signal for input to a pair of DACs, or an interpolating DAC device such as the AD9857(or AD9957). Optionally, the output can be selected as an IF to supply a signal DAC.

The active FEC code-rate and frame structure are automatically decoded from the TLV input stream.

The design has been optimised to provide excellent performance in FPGA devices.

A description of the processing steps follows:

Frame construction. The ISDB-S3 slot and frame structure is formed using the information received over the TLV interface. Slot packet data and TMCC signalling information is sequenced through the encoding chain ready for final mapping and frame building.

Energy Dispersal. The energy dispersal block performs the ISDB-S3 scrambling randomisation polynomial.

BCH, LDPC Encoders. These blocks systematically encode each frame and apply error correction.

Bit Interleaver, Mapping. The bit interleaver block applys block-based bit interleaving to the coded frame prior to symbol mapping.

PL Framing. This block constructs the physical layer framing around the encoded frame data together with the physical-layer frame and slot headers. The PL Framing block is also responsible for the insertion of the encoded TMCC signalling information.

A(PSK) Modulation. This block generates the complex constellation points from the mapped symbol data.

Detailed Description (cont'd)

Rate Conversion. This block re-samples the complex samples output from the A(PSK) Modulation block at symbol-rate into complex samples at the core clock frequency.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external vice that could take separate I/Q, multiplexed I/Q or a single IF output.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Full details of the registers within the modulator core are contained within the full data sheet.

Principle I/O Description

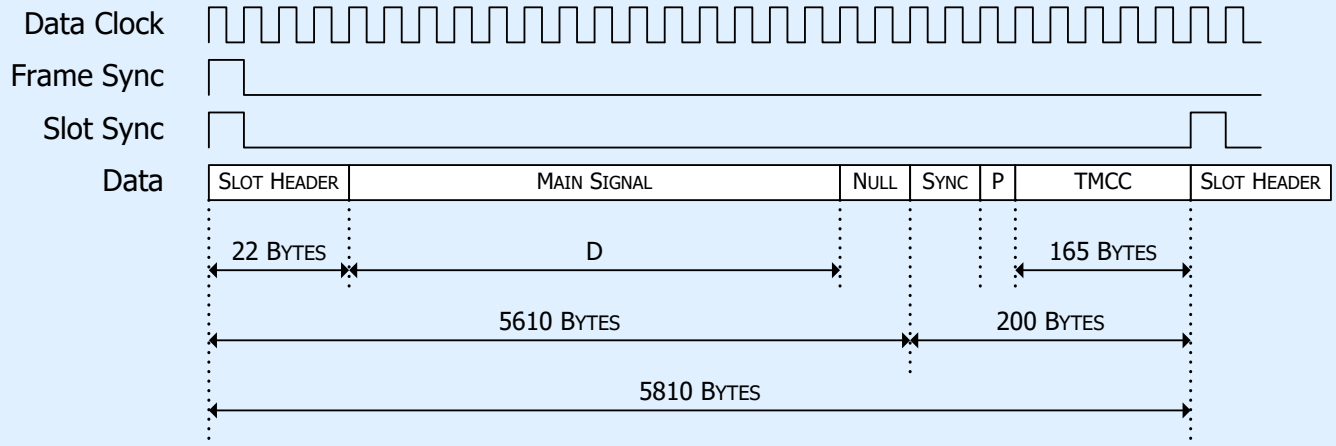
Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0070 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
TLV Interface	
is3_data	8-bit ISDB-S3 TLV data input
is3_data_valid	is2_data data valid input.
is3_slot_sync	ISDB-S3 Slot start sync input.
is3_frame_sync	ISDB-S3 Frame start sync input.
is3_data_clock	ISDB-S3 data clock input.
is3_data_ref_clock	ISDB-S3 clock reference output
Modulator Output Interface	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
Others	
clock	Clock input.
reset_n	Asynchronous active-low reset input.

TLV Interface

Standard interface:

The standard interface supplied accepts a TLV stream input at a rate linked to the on-air modulation rate. To facilitate this, the modulator outputs a reference clock that should be used to clock the TLV data into the core.

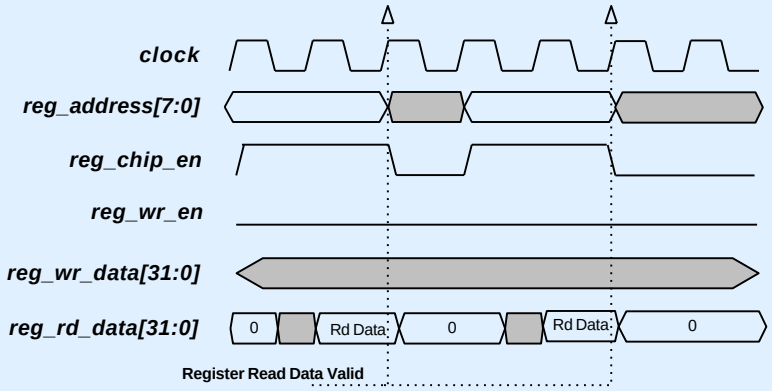
The input stream provides all the information required to construct the ISDB-S3 frame – including slot data, and TMCC slot encoding information.



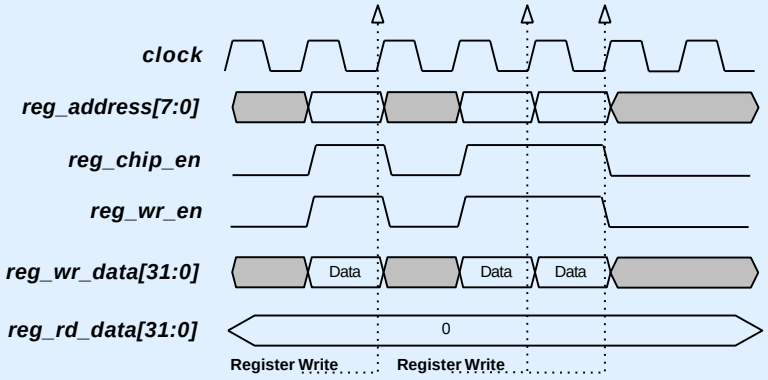
Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC/QSYS builder via the Avalon bus using a zero wait-state configuration.

Register read access:



Register write access:



Altera® Megacore®

AMPP℠ Approved | OpenCore® Support | Qsys Compliant

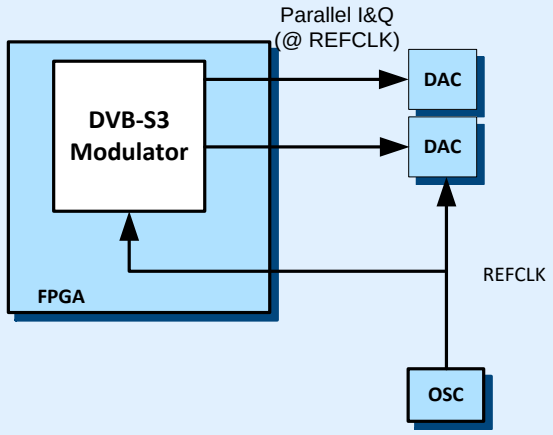
The ISDB-S3 Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.

EXAMPLE APPLICATIONS

Up-sampled output using internal interpolation & up-conversion:

This application uses the ISDB-S3 modulator core with internal interpolation that allows the symbol-rate to be changed via a simple s/w register change.

The ISDB-S3 modulator internal up-conversion is also used which allows direct connection to external DAC devices.



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2/S2X, ISDB-S3, DVB-CID, ATSC-8VSB, ISDB-T, DVB-C/J.83/A/B/C, DVB-T/H and DVB-T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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