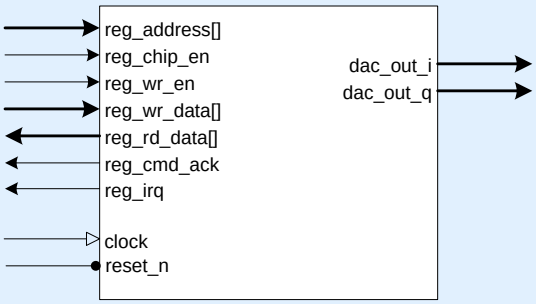
DVB-CID Modulator

CMS0069

- Compliant with ETSI EN 103 129.
- Enables rapid development of carrier identification systems using commodity low-cost FPGAs.
- Provides support for all 32 Content-ID options.
- Individual Content-ID enable options.
- Automatic Content-ID profile sequencing.
- Optional CPU-free configuration.
- Supports all required chip-rates using a single clock reference.
- AD9857/AD9957/AD9789 interface and auto-programming support.
- AD9516/ADF4350 PLL programming support.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



DVB CID®

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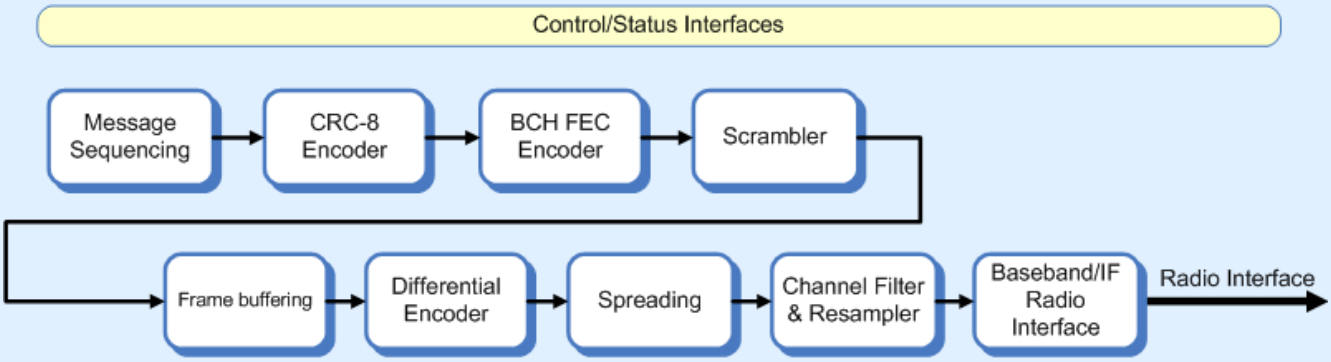
Block Diagram



Detailed Description

The Commsonic CMS0069 DVB-CID Modulator provides all the necessary processing steps to modulate the Content-ID table into a complex I/Q signal for input to a pair of DACs, or interpolating DAC devices such as the AD9857/AD9957 or RF-DACs such as the AD9789. Optionally the output can be selected as an IF to supply a single DAC.

The design has been optimised to provide excellent performance in low cost FPGA devices such as the Cyclone™ range from Altera or the Spartan™ range from Xilinx

A description of the processing steps follows:

Message Sequencing. The software provided hardware Content-ID table is automatically scanned before being output in the required sequence together with the *Unique-Word* as required by the DVB-CID specification. Alternatively, a fixed hardware Content-ID table may be used – further reducing the processing overhead required for the DVB-CID modulator core.

CRC-8 Encoding. An 8-bit CRC is added to each Content-ID packet and serves to allow packet-level error detection at the receiver.

BCH Encoding. Each Content-ID packet is protected through a (127, 85) 6-error correcting systematic BCH code before being scrambled.

Scrambling. All the bits within the DVB-CID frame are scrambled for energy dispersal using the DVB randomisation polynomial $1+x^5+x^9$.

Frame buffering and differential encoding. Each DVB-CID frame is buffered and differential encoded prior to implementation of the spreading algorithm.

Spreading. Each DVB-CID is 'chipped' to the appropriate rate as determined by the host carrier baud-rate, before mapping and channel-filtering.

Resampler. This block re-samples the complex samples output from the channel filter into complex samples at the core clock frequency. This provides an ultra-flexible clocking strategy. This block also scales automatically as required to satisfy the selected chip-rate.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

Detailed Description (cont'd)

DAC Aperture Correction. This optional step provides compensation for the sin(x)/x (or SINC) distortion that is introduced in the DAC. This block may be removed using synthesis options is the feature is not required.

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external vice that could take separate I/Q, multiplexed I/Q or a single IF output.

Additional modes are added to support the Analog Devices AD9857(or AD9957) device that provide up-conversion, SINC filtering and DAC functions in a single package. The AD9857 device requires that the I/Q data be multiplexed onto a single data bus. The *ad9857_pdclk* input is provided to enable this feature and should be sourced from the AD9857 PDCLK output.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Full details of the available registers and control configuration for the modulator core are contained within the full IP guide for the core.

Principle I/O Description

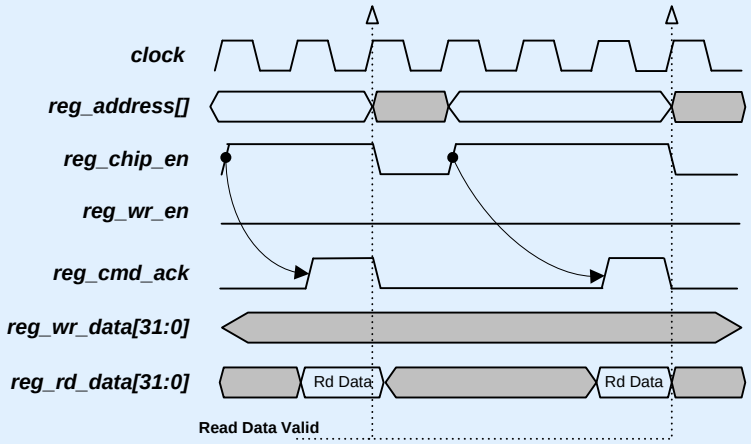
Register Bus Interface	
reg_address (I) []	Register address select input.
reg_chip_en (I)	Active-high block select input for the CMS0069 register bank.
reg_wr_en (I)	Active-high write Enable Input for CMS0069 access.
reg_wr_data (I) [31:0]	32-bit Write data input.
reg_rd_data (O) [31:0]	32-bit Read data output.
reg_cmd_ack (O)	Active-high command acknowledge.
reg_irq (O)	Active-high interrupt line.
Modulator Output Interface	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
ad9857_txdata	14-bit multiplexed data to the AD9857 if used.
ad9857_txenable	Controls the interface timing to the AD9857 if used.
Others	
clock	Clock input, greater than 100MHz for 10MHz bandwidth operation.
ad9857_pdclk	AD9857 Clock.
reset_n	Asynchronous active-low reset input.

Register Interface

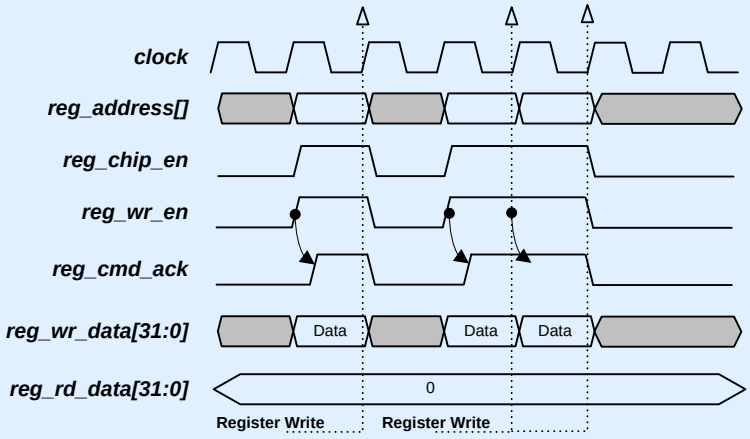
A 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application.

An active-high interrupt line is also available.

Register read access:



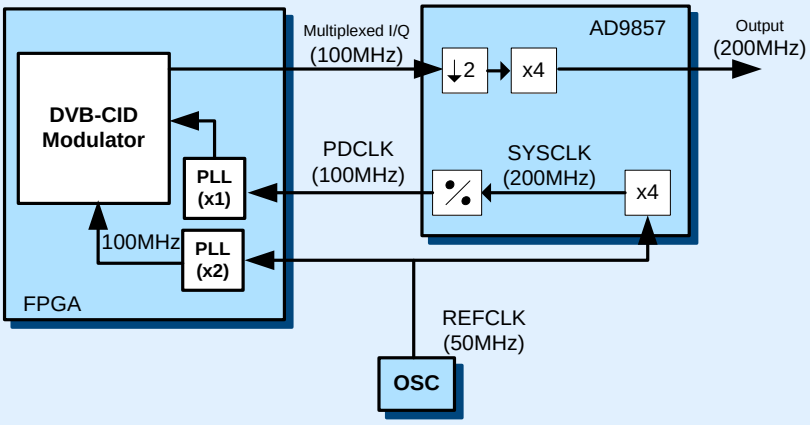
Register write access:



Example Applications

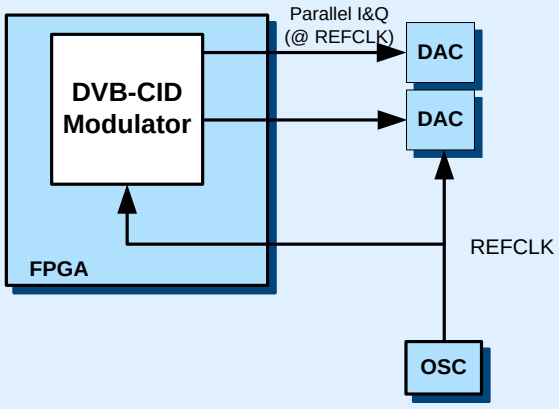
Up-sampled CID output using external up-conversion:

This application uses the DVB-CID modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change.

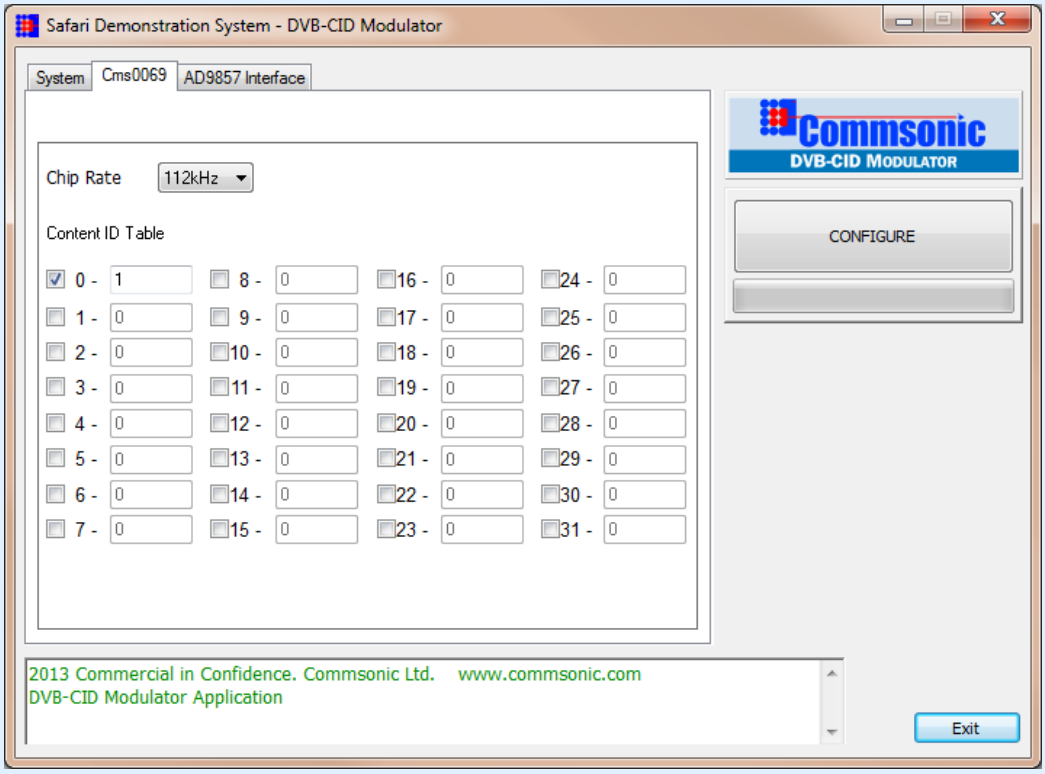


Up-sampled CID output using internal interpolation & up-conversion:

This application uses the DVB-CID modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change. The DVB-CID modulator internal up-conversion is also used which allows direct connection to external DAC devices



Evaluation



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, DVB-CID, ATSC-8VSB, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2 and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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