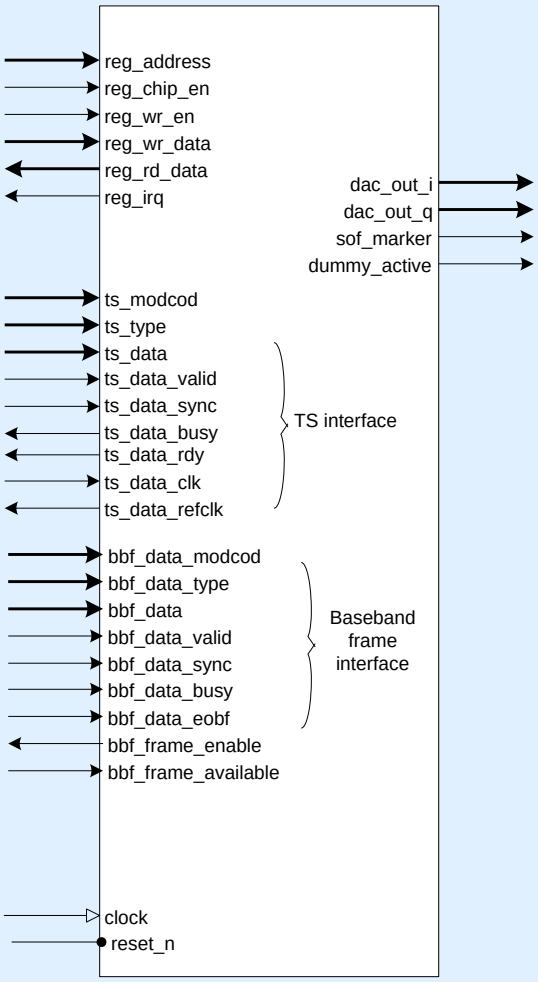
DVB-S2/S2X Modulator

CMS0025

- Fully compliant with ETSI EN 302 307-1 and ETSI EN 302 307-2.
- Variable sample-rate interpolation provides ultra-flexible clocking strategy
- Support for CCM, VCM and ACM modes.
- Optional DVB-S2X VLSNR support
- Compatible with Broadcast, DSNG, Interactive and Professional DVB-S2 and DVB-S2X profiles.
- QPSK, 8-PSK, 16-APSK and 32-APSK supported.
- 64-APSK, 128-APSK and 256-APSK supported.
- Short (16kb) and normal (64kb) frames.
- Frames with/without intra-frame pilots.
- Automatic dummy-frame insertion.
- Support for VLSNR frames and encoding.
- Integrated LDPC channel coder.
- Optional simultaneous DVB-CID modulation.
- Configurable for either low-latency or high-throughput encoding.
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping.
- Seamless integration with Altera ASI megacore when using SPI/ASI extension core in broadcast CCM mode.
- Optional internal IF conversion.
- Optional noise interference source.
- AD9857/AD9957 interface and auto-programming support.
- Modes that are not required may be removed with synthesis options to generate a compact, efficient design.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).

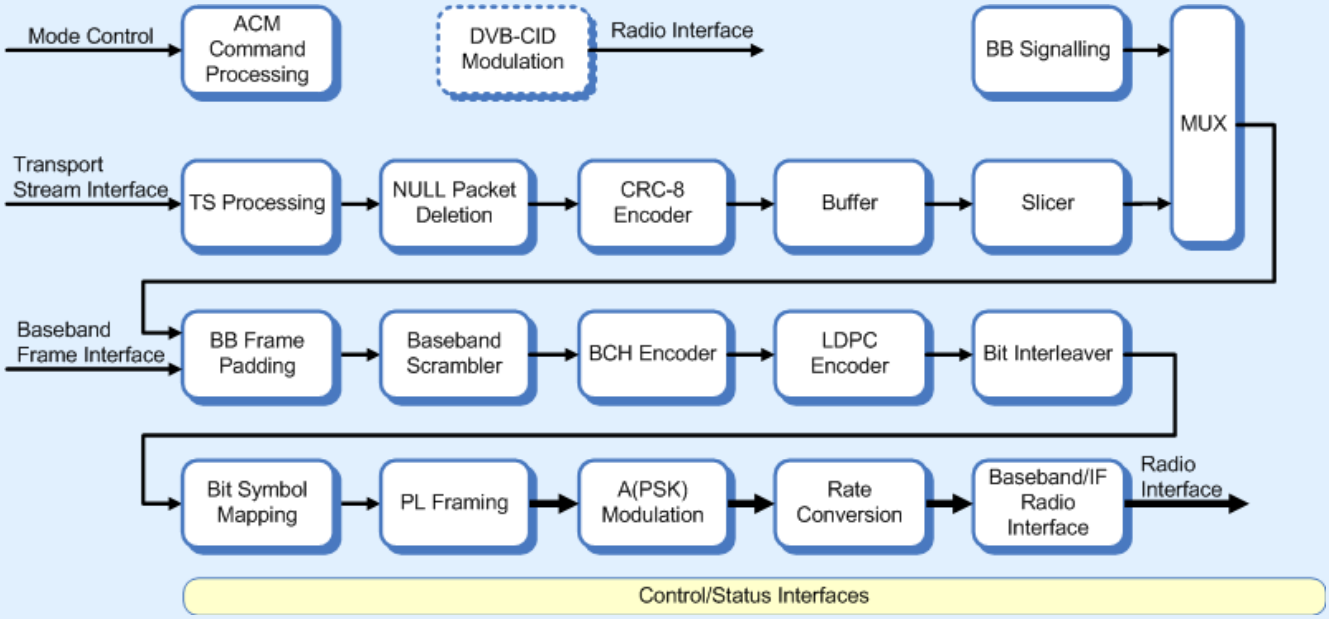


Contact information

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845

Block Diagram



Detailed Description

The Commsonic CMS0025 DVB-S2/S2X Modulator with integrated LDPC encoder has been designed specifically to address the requirements of the ETSI DVB-S2 forward-link satellite standard (EN 302 307), section-1 together with the section-2 extensions (DVB-S2X), with additional support for DVB-S2X VLSNR operation. The core can operate in CCM and VCM/ACM modes.

The core provides all the necessary processing steps to modulate a single transport stream (or baseband-frame) into a complex I/Q signal for input to a pair of DACs, or an interpolating DAC device such as the AD9857(or AD9957). Optionally, the output can be selected as an IF to supply a signal DAC.

The active FEC code-rate and frame-size are defined by the mod_cod and type parameters associated with each TS packet (or input-frame) and are controlled through the external mode control ports, or optionally from a control register for CCM applications.

The design has been optimised to provide excellent performance in FPGA devices.

A description of the processing steps follows:

TS Processing. The TS processing block performs rate adaptation functions in CCM Broadcast applications to ensure that variable transmission delays do not result in disturbances of time-critical services such as audio and video.

Null packet deletion. The Null packet deletion block removes null TS packets from the input stream to maximise the capacity available for information services in VCM and ACM modes. The mechanism defined by DVB-S2 allows for complete restoration of the input stream when null packets are necessary to maintain a constant delay.

CRC-8 Encoding. An 8-bit CRC is added to each outgoing TS packet and serves to allow packet-level error detection at the receiver.

Slicer. The slicer block assembles each output BBFRAME from an integer number of TS packets. Padding may be used at the end of the BBFRAME if the number of bits is not exactly an integer number of TS packets. In VCM/ACM applications a new BBFRAME is initiated whenever the MODCOD or TYPE are modified. If this occurs before the end of an outgoing BBFRAME then the outgoing frame is padded.

Baseband Signalling. The baseband signalling block inserts a fixed-length Baseband Header at the start of each BBFRAME. The structure of the Baseband Header is as described in EN 302 307.

Baseband Scrambler. The baseband scrambler block performs the energy dispersal and transport multiplex adaptation using the DVB randomisation polynomial $1+x^{14}+x^{15}$.

Detailed Description (cont'd)

BCH, LDPC Encoders. These blocks systematically encode each frame and apply error correction.

Bit Interleaver, Mapping. The bit interleaver block applys block-based bit interleaving to the coded frame prior to symbol mapping.

PL Framing. This block constructs the physical layer framing around the encoded frame data together with the physical-layer header. The PL Framing block is also responsible for intra-pilot insertion together with dummy-frame generation

A(PSK) Modulation. This block generates the complex constellation points from the mapped symbol data.

Rate Conversion. This block re-samples the complex samples output from the A(PSK) Modulation block at symbol-rate into complex samples at the operating clock frequency. This provides an ultra-flexible clocking strategy allowing the core to operate from low symbol-rates up to a maximum of twice the core clock frequency.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external vice that could take separate I/Q, multiplexed I/Q or a single IF output.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Full details of the registers within the modulator core are contained within the full data sheet.

Principle I/O Description

Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0025 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
Transport Stream Interface	
ts_data	8-bit Transport Stream data input
ts_data_valid	Transport Stream data valid input.
ts_data_sync	Transport Stream data sync input.
ts_data_rdy	Transport Stream data interface ready output.
ts_data_busy	Transport Stream interface busy output. TS data should be stalled until the interface is available again. (Only relevant to ACM operation when using the TS PCR plug-in).
ts_data_clk	Transport Stream clock input.
ts_data_refclk	Transport Stream reference clock output.
ts_modcod	Defines FEC code-rate and modulation for the current Transport Stream packet.
ts_type	Defines the frame size and inclusion of intra-frame pilots for the current Transport Stream packet.
Baseband Frame Interface	
bbf_data	8-bit baseband frame data input
bbf_data_valid	Baseband frame data valid input.
bbf_data_sync	Active-high input flag indicating the first data of the frame.
bbf_data_busy	Active-high output flag indicating that core is busy and cannot accept any more data.
bbf_data_eobf	Active-high input flag indicating that this is the final byte of the frame.
bbf_frame_enable	Active-high output flag indicate that this interface has gained access to the modulation chain, and the frame should be input.
bbf_frame_available	Active-high input flag indicating that there is a frame ready to be input.
bbf_data_modcod	Defines FEC code-rate and modulation for the current baseband frame.
bbf_data_type	Defines the frame size and inclusion of intra-frame pilots for the current baseband frame.

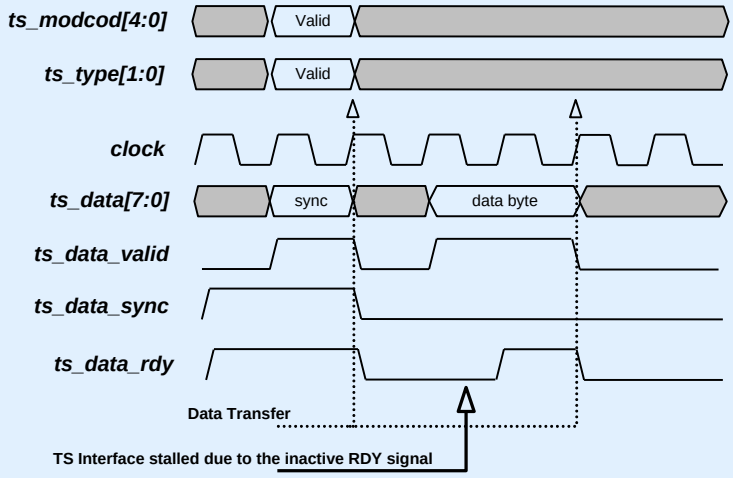
Principle I/O Description (cont'd)

Modulator Output Interface	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
dummy_active	Active-high flag indicating that a dummy-frame is being transmitted.
sof_marker	Active-high flag indicating the start of the transmission for a frame.
Others	
clock	Clock input, greater than 2x maximum supported symbol-rate.
reset_n	Asynchronous active-low reset input.

Transport Stream Interfaces

Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism to allow data to be pulled through the modulator processing chain based on the on-air symbol rate. This requires the TS data source to be stalled when the modulator core is busy.



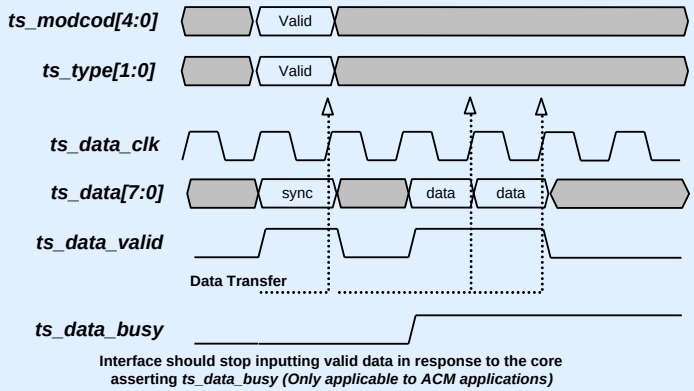
PCR re-stamping TS interface:

Typically for CCM broadcast applications, the input stream from the transport multiplexer is provided at a fixed rate that requires 'padding' to match the required on-air bitrate. For this application, the Null-Packet-Deletion block cannot be used, and consequently some form of traditional MPEG TS rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate.

The core will be pad the input TS stream with NULL TS packets as required and perform any PCR adjustment.

When the PCR restamping extension core is used, an output signal, *ts_data_refclk* is provided that indicates the necessary 188-byte TS byterate to satisfy the on-air requirements for broadcast CCM operation.

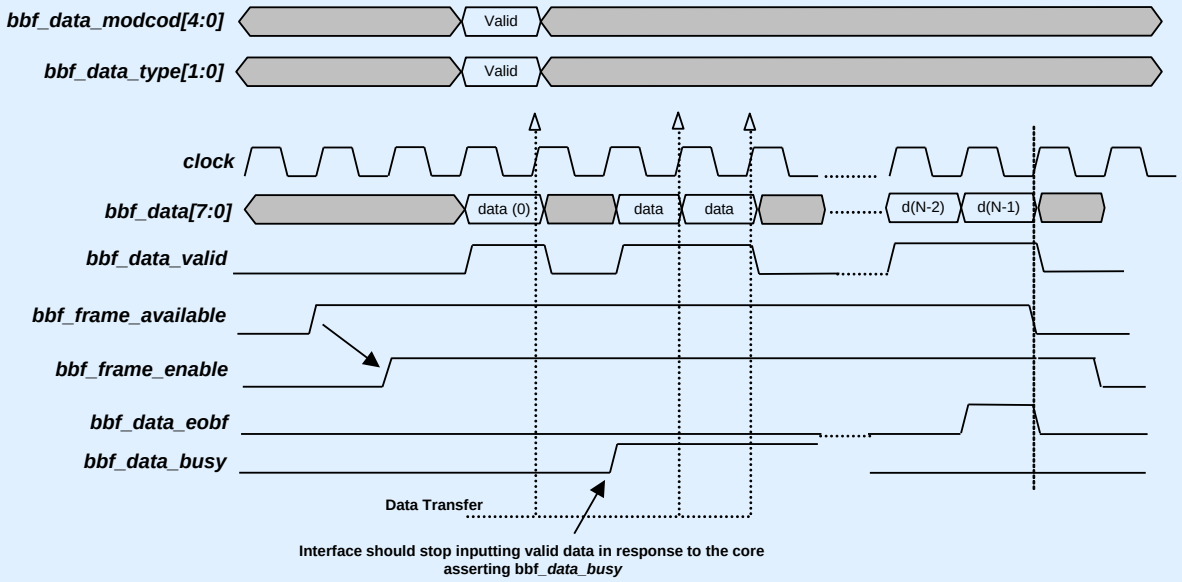
For ACM applications the core generates an additional output signal, *ts_data_busy*. The input TS stream should be stalled whilst *ts_data_busy* is high. This allows data to be burst into the core at a higher bitrate. Following the assertion of *ts_data_busy*, the core can accept 3 more input bytes before the cores input buffers are overflowed.



Baseband frame interface

Other applications may require additional baseband frame (BBFRAME) processing over and above those supplied with the Transport Stream Interface. For such applications, the core provides a baseband frame interface that accepts external constructed BBFRAMEs before encoding, physical layer construction and modulation.

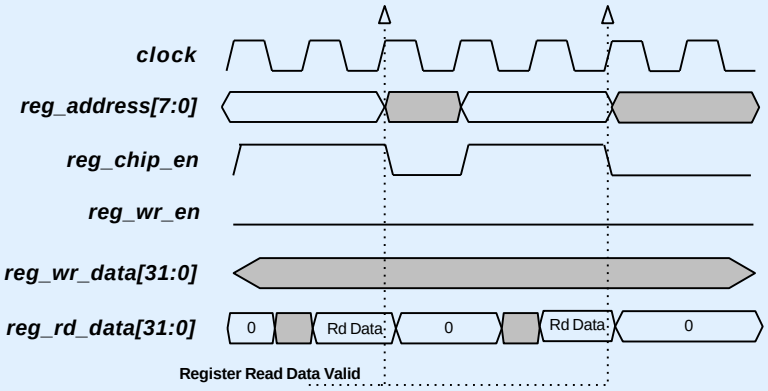
The baseband frame interface uses a valid/busy handshake mechanism to allow data to be pulled through the modulator processing chain based on the required on-air symbol rate. This requires the frame data source to be stalled when the modulator core is busy. Conversely, the modulator core can insert dummy-frames when a constructed frame is not available.



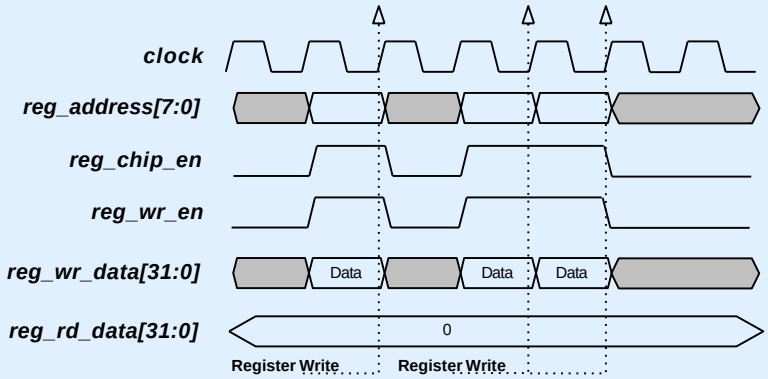
Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC/QSYS builder via the Avalon bus using a zero wait-state configuration.

Register read access:



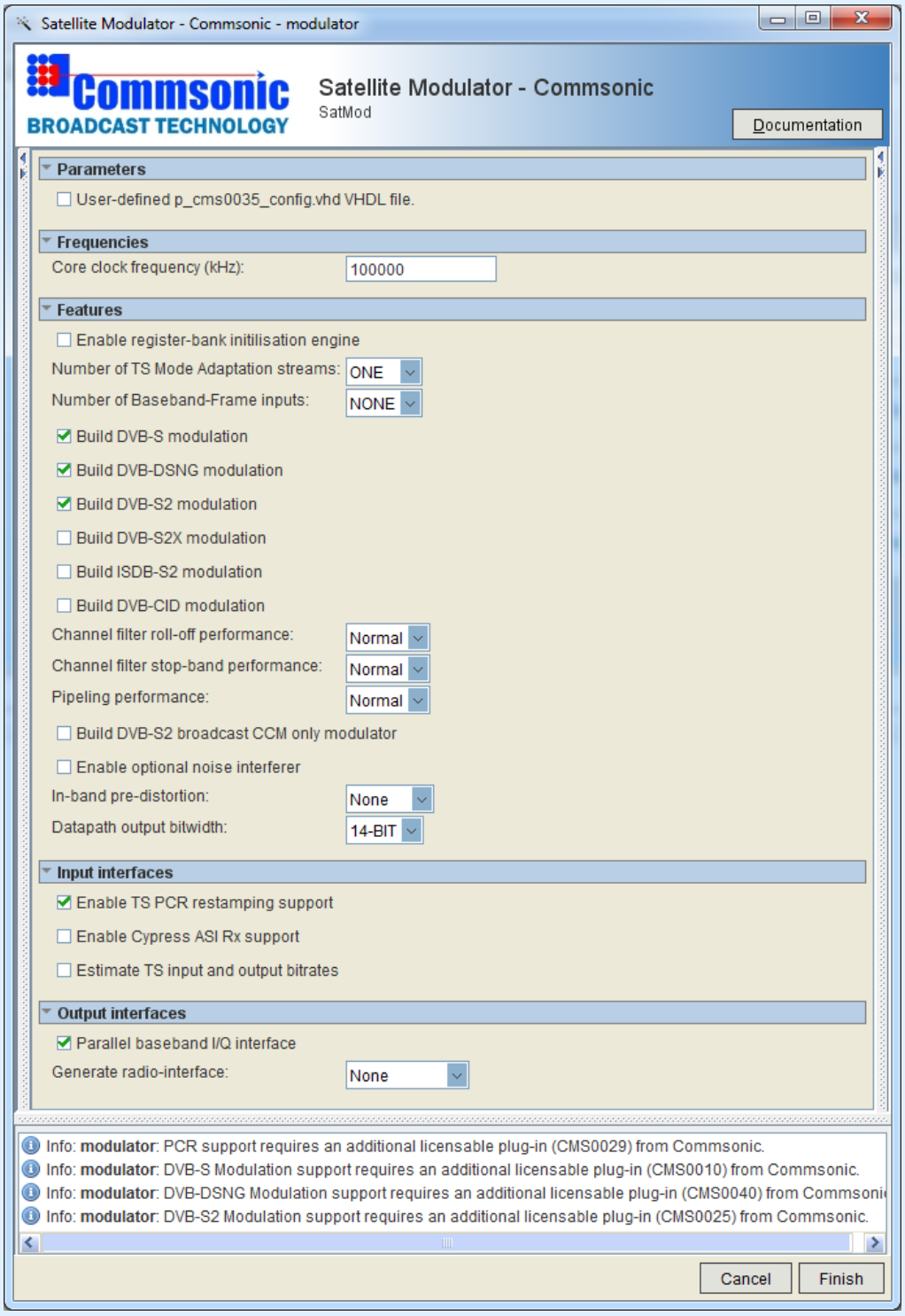
Register write access:



Altera® Megacore®

AMPP℠ Approved | OpenCore® Support | Qsys Compliant

The DVB-S2/S2X Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.

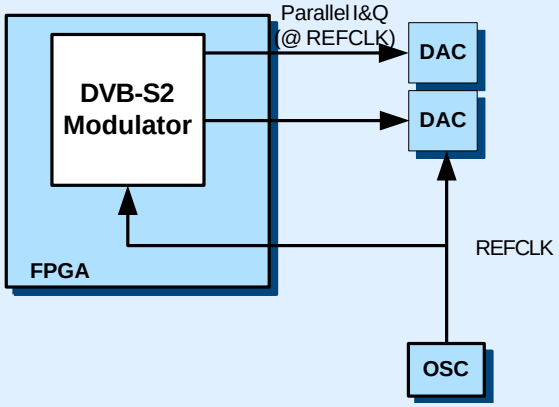


EXAMPLE APPLICATIONS

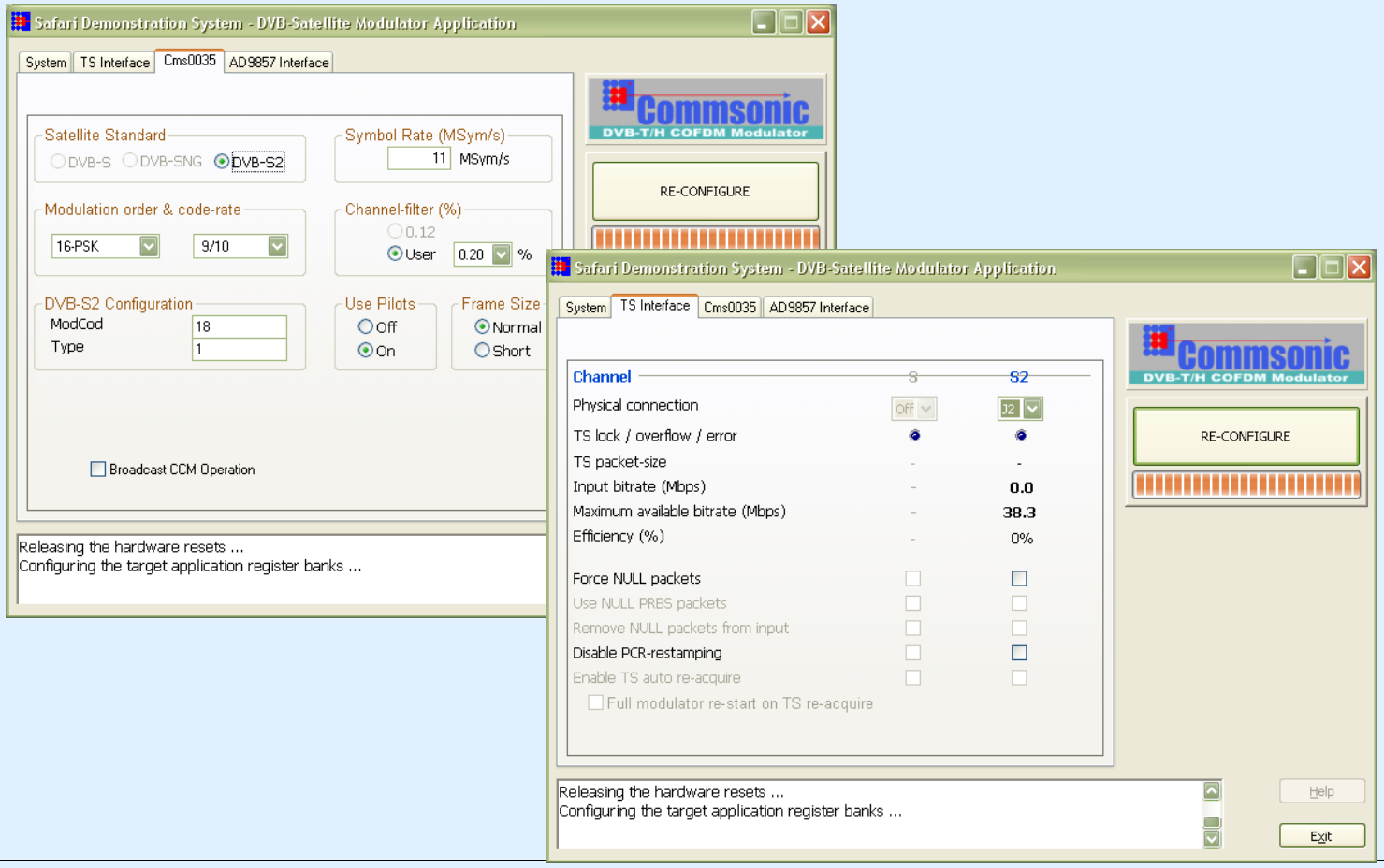
Up-sampled output using internal interpolation & up-conversion:

This application uses the DVB-S2(X) modulator core with internal interpolation that allows the symbol-rate to be changed via a simple s/w register change.

The DVB-S2(X) modulator internal up-conversion is also used which allows direct connection to external DAC devices



EVALUATION



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2/S2X, ISDB-S2, DVB-CID, ATSC-8VSB, ISDB-T, DVB-C/J.83/A/B/C, DVB-T/H and DVB-T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845