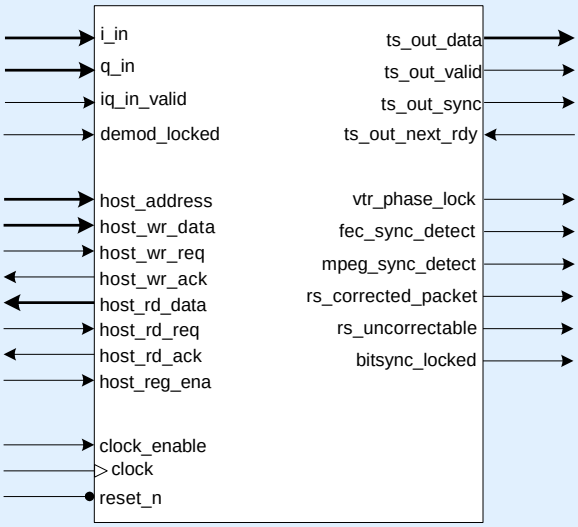
# J.83abc/DVB-C Cable FEC Decoder

## CMS0018

- Provides the required channel coding functions for cable television as specified by ITU Recommendation J.83 Annexes ABC and DVB-C.
- Configurable I/Q input width
- Standard 188-byte MPEG Transport Stream output.
- C / C++ header file defines Host Interface registers, allowing software mode control.
- External RAM interface for long interleave modes.
- Synthesis control to build for any subset of the supported modes, removing unneeded logic.
- Optional BER monitor provides statistics on Errors Corrected and Residual Packet Errors.

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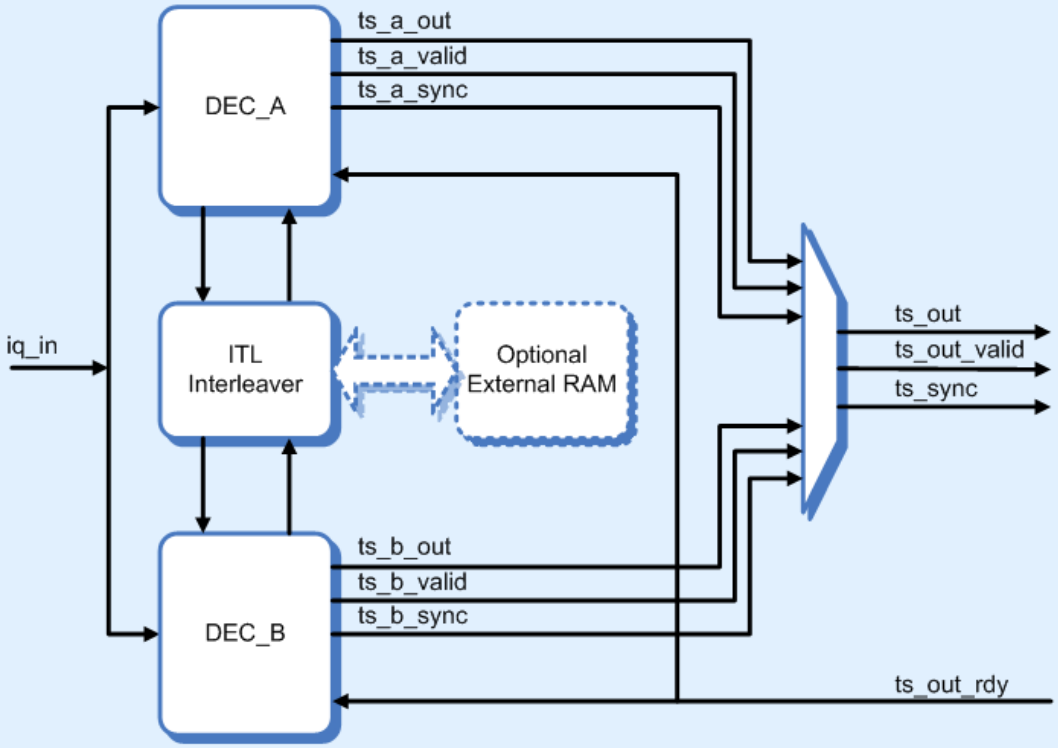
## Block Diagram




## Detailed Description

The Commsonic CMS0018 J.83abc/DVB-C Cable FEC Decoder combines all of the channel coding and Forward Error Correction functions specified by DVB-C and by J83 – Annexes A B and C

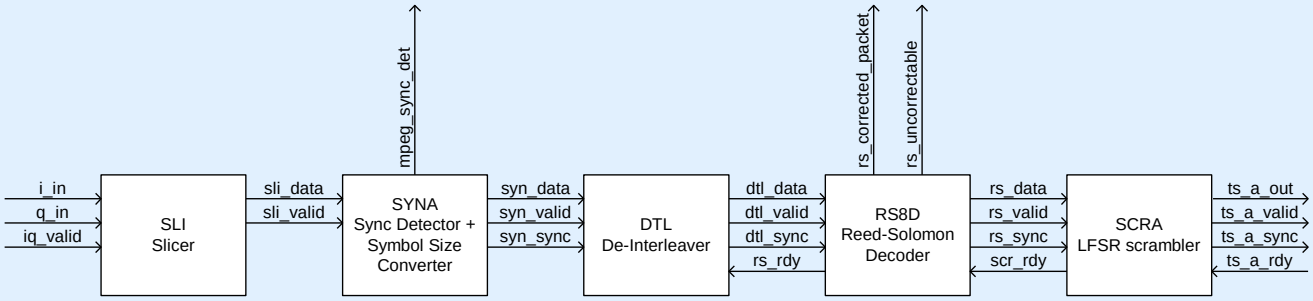
The CMS0018 includes functions for QAM constellation slicing, trellis decoding, de-framing, de-scrambling, de-interleaving, and Reed-Solomon decoding.

With the exception of the common de-interleaver block, two independent datapaths are required. J83A J83C and DVB-C are quite similar in requirements. These are implemented in the DEC_A sub-block

The requirements of J83 Annex B are significantly different. The largest difference is the addition of trellis coding, but the Reed-Solomon code is also uniquely different and the scrambler is based on a different algorithm. In practice, only the de-interleave block may be easily shared between them.

# Detailed Description (Cont'd)

## DEC_A (DVB-C and J.83 Annex A + C)



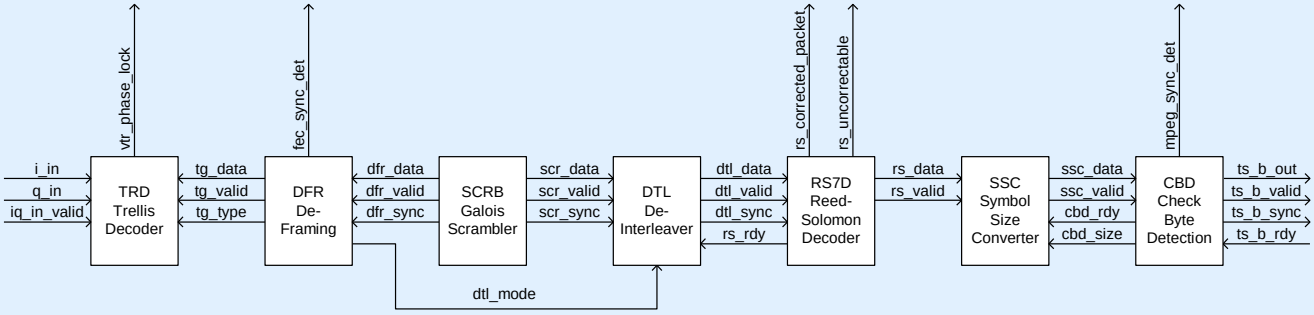

The DEC_A sub-block supports the full set of DVBC constellations, of which J.83 Annex A and C are subsets. This includes 16-, 32-, 64-, 128- and 256-QAM.

These modes use a single interleave configuration.

Mode control is provided via the host interface registers. Annex A/C-mode is selected by setting the ***AnnexBEnable*** register = 0.

The number of bits per symbol is set by ***QamMode*** = bits_per_symbol – 4

## DEC_B (J.83 Annex B)




The DEC_B sub-block supports J.83 Annex B.

Incoming IQ samples from the demodulator are first Trellis Decoded. Viterbi puncture alignment is found by searching all possible data phases and comparing error rates. Once the correct phase is found,the `vtr_phase_locked` status flag goes high.

Valid data bits from the Trellis Decoder are then searched for framing alignment. The frame sync field indicates alignment for both De-scrambler and Reed-Solomon decoder.

The sync field also includes the four-bit Interleave Mode. The De-Interleaver supports the full set of J.83 B modes, but there is a synthesis option for the short (128x1) modes specified for DOCSIS 1.0 and 1.1, reducing memory requirements by a factor of eight.

The 7-bit De-Framed symbols are De-Scrambled, De-Interleaved and RS decoded.

The SSC converts 7-bit Reed-Solomon outputs into bytes. Phase alignment is guided by Check Byte Detection. The J83B Encoder replaces the 0x47 MPEG sync byte with a checksum. All possible phases are searched until checksum match is found. The checksum bytes are then replaced with 0x47 and the resulting TS packets output. The **`mpeg_sync_detect`** flag indicates error-free TS packets.

## Principle I/O Description

| Host Interface | |
|---|---|
| host_addr | 8-bit register address |
| host_reg_ena | Active high enable (chip select) Must be high for read or write access. |
| host_wr_data | 8-bit RAM write data |
| host_wr_req | 1 => write cycle request (write data valid) |
| host_wr_ack | 1 => write cycle acknowledge. Because there is no internal arbitration for RAM, CMS0017 always accepts write data and this output is always true. |
| host_rd_data | 8-bit RAM read data |
| host_rd_req | 1 => read cycle request. Must be held high until **host_rd_ack** = 1. |
| host_rd_ack | 1 => read cycle acknowledge (read data valid). This signal indicates that read data is valid. Goes high one cycle after **host_rd_req**. |
| **Decoder Interface** | |
| i_in | In-phase portion of demodulated constellation (two's complement)<br>Width is specified by fec_iq_input_bits generic |
| q_in | Quadrature portion of demodulated constellation. |
| iq_in_valid | Indicates current input symbol is valid. |
| demod_locked | Indicates the demodulator thinks it has acquired a valid signal.<br>This initiates FEC acquisition mode. |
| ts_out_data | Decoded Transport Stream data bytes |
| ts_out_valid | 1 => decoded data and sync outputs are valid |
| ts_out_sync | 1 => current output byte is first in TS packet (0x47) |
| ts_out_next_rdy | 1 => Next block in decoder chain is ready for new TS data byte.<br>Data transfer occurs when ts_out_next_rdy = ts_out_valid = 1 |

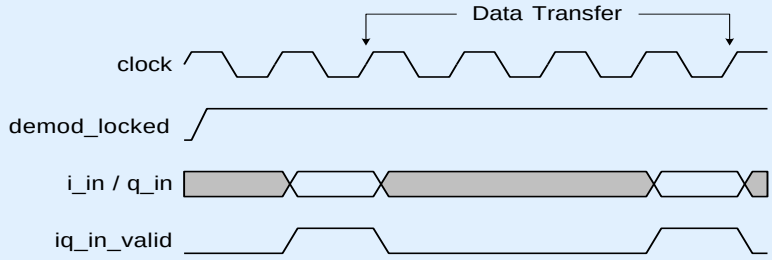
## Principle I/O Description (Cont'd)

| | |
|---|---|
| **Status Outputs** | |
| vtr_phase_lock | Indicates the Trellis Decoder has determined the correct Viterbi puncture phase<br>Only used with J83 Annex B |
| fec_sync_detect | In Annex A/C mode, Indicates 188-byte MPEG sync has been detected.<br>In Annex B mode, indicates FEC frame alignment detection |
| mpeg_sync_detect | Indicates 188-byte MPEG sync has been detected.<br>In Annex A/C mode, this is the same as fec_sync_detect. |
| Rs_corrected_packet | Indicates the selected RS decoder has corrected errors. |
| Rs_uncorrectable | Indicates the selected RS decoder has found an uncorrectable packet |
| bitsync_locked | This is a mode-dependent composite signal based on the above status outputs. This is intended to control demodulator acquisition mode. When bitsync_locked is low, the demodulator should re-acquire. |
| **External Memory Interface** | |
| dtl_ram_addr | 16-bit ram address |
| dtl_wr_ena | Active high RAM write enable |
| dtl_wr_data | 8-bit RAM write data |
| dtl_rd_data | 8-bit RAM read data |
| **Others** | |
| clock | Clock Input |
| reset_n | Asynchronous reset input (active low) |
| clock_enable | This is actually a logic enable. Logic results are captured on the rising clock edge when clock_enable = 1. |

# Timing Diagrams

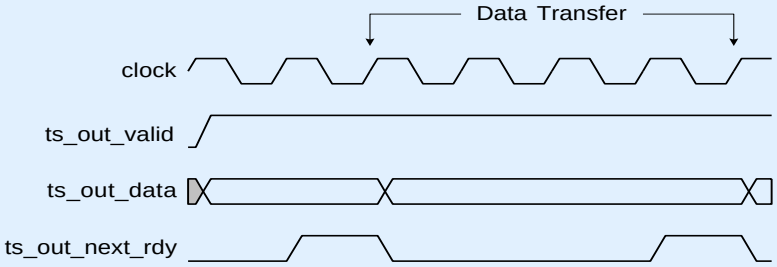
## QAM Symbol Input:

The input data interface is designed to accept data at a minimum of four clocks per byte.



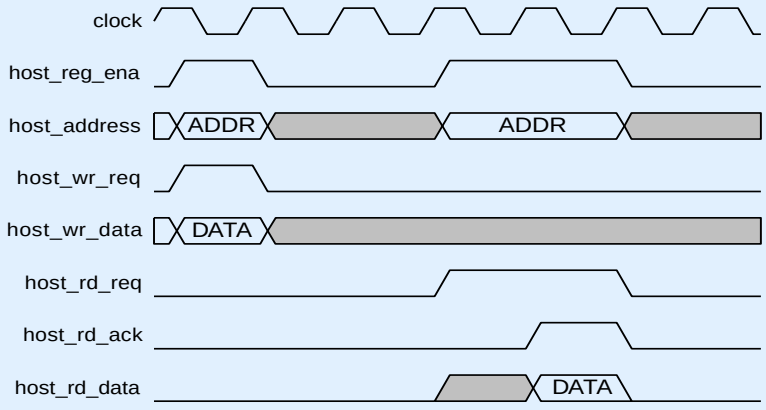

## Transport Stream Output:

The output data interface is implemented with RDY-VALID handshaking. This provides a simple interface in which each block may moderate the data flow to match its own data processing requirements. The data source asserts its VALID flag when it presents data. The data destination indicates availability using its RDY flag. Data transfer occurs synchronously when both the source's VALID and the destination's RDY = 1.




## Host Interface:

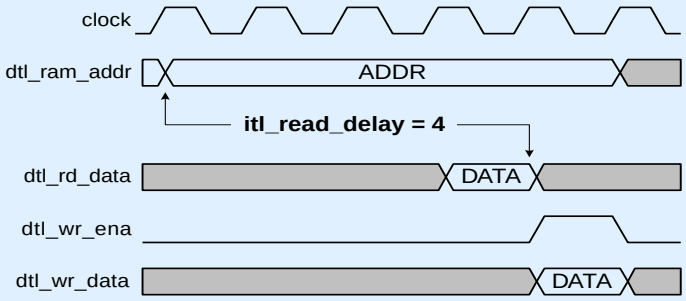
The Host Interface is synchronous with the system clock input. The REQ – ACK handshake is similar to the RDY-VALID handshake used for the TS data interface.



# Timing Diagrams (Cont'd)

## External Memory Interface:

The CMS0018 may be configured to use memory external to the core. The timing of this interface is controlled by the synthesis constant **`itl_read_delay`**, illustrated below.



## Host Interface Registers

The host interface registers allow software to control the encoder's mode of operation. For programming convenience, the CMS0018 package includes a standard C / C++ header file defining the host register bank as a structure. The members of that structure are as follows:

| Name | Address | Description |
|---|---|---|
| SoftReset | 0x00 | Write 1 to this register to force all internal states to reset. Remaining register contents are unaffected. This register dafults to 1 on hardware reset, so a zero must be written here to enable the core. |
| Version | 0x04 | This read-only register returns the version number of the core. |
| AnnexBEnable | 0x08 | 1 => Annex B mode. 0 => Annex A+C+DVBC |
| QamMode | 0x0C | Specifies the number of bits per symbol :<br>*QamMode* = bits_per_symbol – 4 |
| ItlMode | 0x10 | When in Annex B mode, this read-only register returns the Interleave mode as extracted from the received data stream. This value is encoded as set out in Recommendation J.83 Annex B : |
| AllowAllSyncPhases | 0x14 | 1 => the Annex A/C Symbol Size Converter allows all possible phases of byte-to-symbol alignment. 0 => only specified alignments are allowed. |
| ReSync | 0x18 | Writing 1 to this self-clearing register forces the Annex B datapath to re-acquire. |
| SyncStatus | 0x1C | This register allows real-time reading of the receive status outputs. In addition, the MSBs are "sticky" bits which show if there has ever been an error condition. Any write to this register will clear the sticky bits.<br>Bit 7 Sync Lost : indicates bitsync_locked has gone low<br>Bit 6 Errors Seen : indicates the TS output has contained errors<br>Bit 5 Bitsync Locked : the decoder will re-acquire automatically<br>Bit 4 MPEG Sync Detect<br>Bit 3 RS Zero Errors : no errors at RS input (not rs_corrected_packet)<br>Bit 2 RS Codeword Found : valid RS codeword (not rs_uncorrectable)<br>Bit 1 FEC Sync Detect : Annex B framing locked / Annex A MPEG detect<br>Bit 0 Annex B Trellis Decoder has achieved Viterbi puncture phase lock. |

## Synthesis Parameters

Build parameters are defined in a VHDL package and applied to the design as GENERICs. These are fixed at synthesis time.

| Name | Description | Default |
|---|---|---|
| build_soft_reset | Selects whether to build a software reset under host control | TRUE |
| build_clock_enable | Selects whether to build the clock_enable logic | TRUE |
| build_external_dtl_ram | Selects whether to build the external RAM interface (TRUE) or instantiate internal RAM (FALSE). | FALSE |
| itl_read_delay | Specifies the number of clock cycles from valid itl_ram_addr until itl_rd_data is latched internally. Default value for local synchronous ram is 2 | 2 |
| build_docsis_itl | Builds only the short Annex B interleave modes (up to 128x1) for DOCSIS 1.0 and 1.1. Reduces memory requirement by 8x. | FALSE |
| fec_iq_input_bits | Width of I/Q inputs. In Annex B mode, the Viterbi soft-decision width is<br>fec_iq_input_bits – 4. | 8 |
| build_j83_a | Selects whether to build support for J.83 Annex A | TRUE |
| build_j83_b | Selects whether to build support for J.83 Annex B | TRUE |
| build_j83_c | Selects whether to build support for J.83 Annex C | TRUE |
| build_dvb_c | Selects whether to build support for DVB-C | TRUE |
| build_docsis_itl | If true, only the shorter Annex B interleave modes are built in accordance with DOCSIS 1.0 and 1.1. Note that DOCSIS 2.0 and 3.0 specify the full range of Annex B modes. | FALSE |
| host_addr_width | Width of the host address bus | 8 |
| host_data_width | Width of the host data bus | 8 |
| build_output_smoothing | FALSE => build the core with a ready-valid interface on the Transport Stream output. TRUE => the TS output is self timed at the correct output byte rate. The ts_out_next_rdy input is ignored. | FALSE |
| build_ber_measurement | Build counters for pre-Viterbi BER, pre-RS BER and Packet Errors | FALSE |

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## About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/S2/DSNG, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2, ATSC and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

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