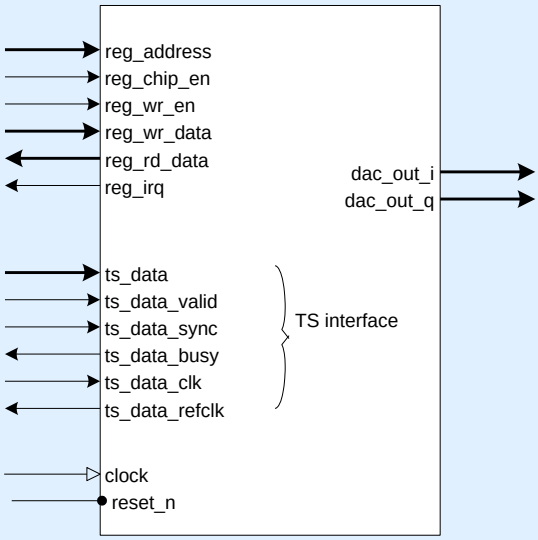
DVB-S/-DSNG Modulator

CMS0010

- Fully compliant with ETSI EN 300 421 and ETSI EN 301 210.
- Variable sample-rate interpolation provides ultra-flexible clocking strategy.
- Integrated DVB-S channel coder.
- Optional DVB-DSNG support.
- Extension core available for SPI/ASI interface with integrated PCR TS re-stamping.
- Seamless integration with Altera ASI megacore when using SPI/ASI extension core.
- Optional internal IF conversion.
- Optional noise interference source.
- AD9857/AD9957 interface and auto-programming support.
- Modes that are not required may be removed with synthesis options to generate a compact, efficient design.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).



Contact information

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845

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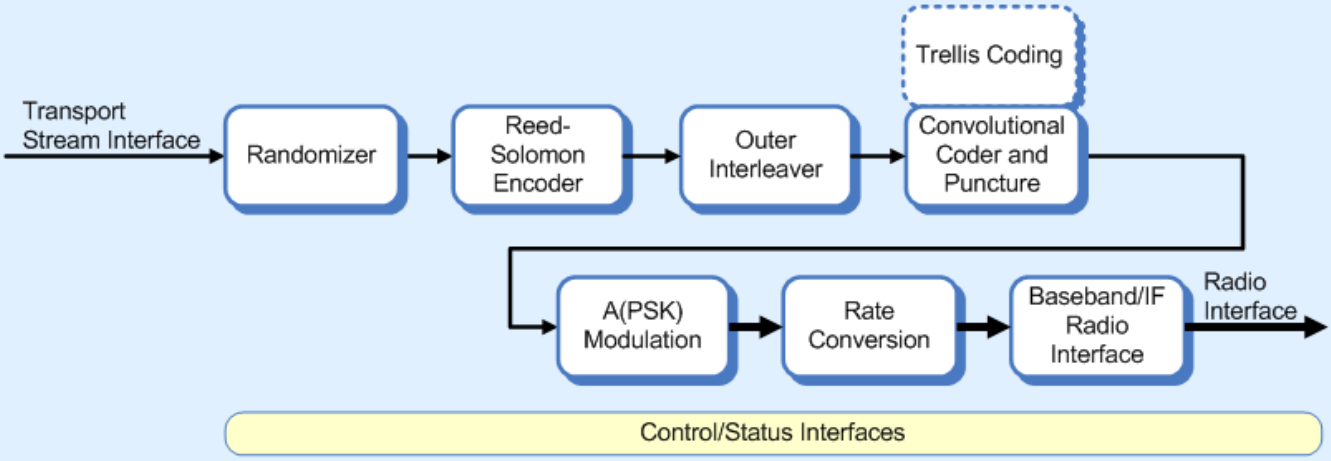
Block Diagram



Detailed Description

The Commsonic CMS0010 DVB-S/-DSNG Modulator with integrated Reed-Solomon encoder has been designed specifically to address the requirements of the ETSI DVB-S forward-link satellite standard (EN 300 421), with further options available for compatibility with the ETSI DVB-DSNG digital satellite news gathering standard (EN 301 210).

The core provides all the necessary processing steps to modulate a single transport stream into a complex I/Q signal for input to a pair of DACs, or an interpolating DAC device such as the AD9857. Optionally, the output can be selected as an IF to supply a signal DAC.

The active FEC code-rate is controlled via a control register.

The design has been optimised to provide excellent performance in FPGA devices.

A description of the processing steps follows:

Randomiser. This block performs the energy dispersal and transport multiplex adaptation using the DVB randomisation polynomial $1+x^{14}+x^{15}$ and also by inverting every eighth sync byte.

Reed-Solomon Encoder. This block generates Reed Solomon packets based on the DVB RS(204, 188) code with code generator polynomial:

$$g(x) = (x+\lambda^0)\,(x+\lambda^1)\,(x+\lambda^2)\ldots\,(x+\lambda^{15})$$

Where λ = 0x02, and field generator polynomial:

$$p(x) = x^8 + x^4 + x^3 + x^2 + 1$$

Outer Interleaver. This block performs the DVB outer interleaving function with depth I=12 as specified by the DVB standard.

Convolutional Encoder. This block performs the convolutional encoding as specified by DVB.

Trellis Coding. This block performs the pragmatic trellis encoding as specified by DVB DSNG standard.

A(PSK) Modulation. This block generates the complex constellation points from the mapped symbol data.

Rate Conversion. This block re-samples the complex samples output from the A(PSK) Modulation block at symbol-rate into complex samples at the core clock frequency. This provides an ultra-flexible clocking strategy allowing the core to operate from low symbol-rates up to a maxium of half the core clock frequency.

Baseband-to-IF. This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

Detailed Description (cont'd)

Radio Interface. This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external vice that could take separate I/Q, multiplexed I/Q or a single IF output.

Register Bank. The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Full details of the registers within the modulator core are contained within the full data sheet.

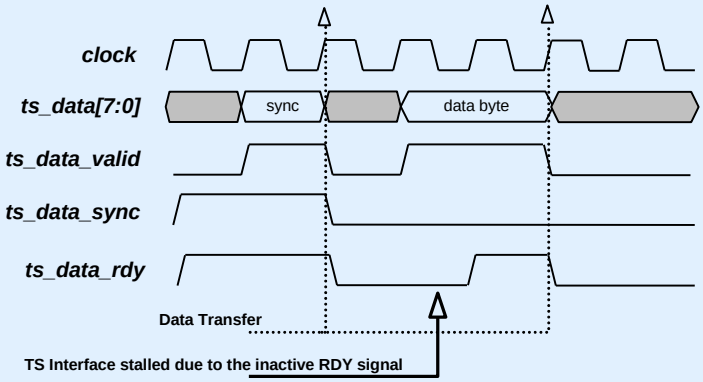
Principle I/O Description

Register Bus Interface	
reg_address	Register address select input.
reg_chip_en	Block select input for the CMS0025 register bank.
reg-wr_en	Write Enable Input for block registers.
reg_wr_data	32-bit Write data input.
reg_rd_data	32-bit Read data output.
reg_irq	Core Interrupt.
Transport Stream Interface	
ts_data	8-bit Transport Stream data input
ts_data_valid	Transport Stream data valid input.
ts_data_sync	Transport Stream data sync input.
ts_data_rdy	Transport Stream interface is ready to accept new TS data.
ts_data_clk	Transport Stream clock input.
ts_data_refclk	Transport Stream reference clock output.
Modulator Output Interface	
dac_out_i	14-bit Transmit I complex output or IF output in IF mode.
dac_out_q	14-bit Transmit Q complex output.
Others	
clock	Clock input, greater than 2x maximum supported symbol-rate.
reset_n	Asynchronous active-low reset input.

Transport Stream Interface

Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism to allow data to be pulled through the modulator processing chain based on the on-air symbol rate. This requires the TS data source to be stalled when the modulator core is busy.

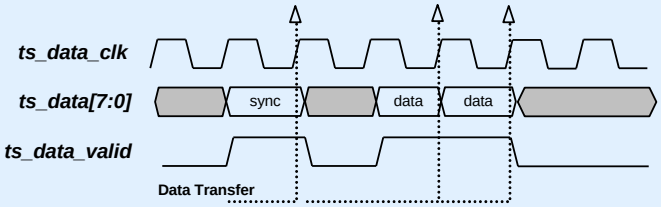


PCR re-stamping TS interface:

Typically for broadcast applications, the input stream from the transport multiplexer is provided at a fixed rate that requires 'padding' to match the required on-air bitrate, and consequently some form of traditional MPEG TS rate adaption is required. The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate.

The core will be pad the input TS stream with NULL TS packets as required and perform any PCR adjustment.

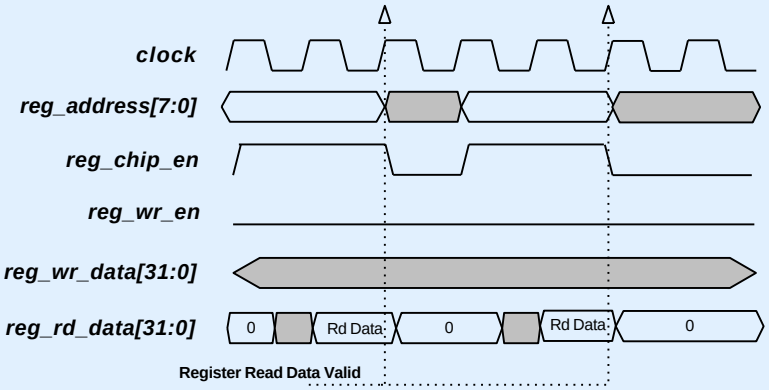
When the PCR restamping extension core is used, an output signal, *ts_data_refclk* is provided that indicates the necessary 188-byte TS byterate to satisfy the on-air requirements for broadcast operation.



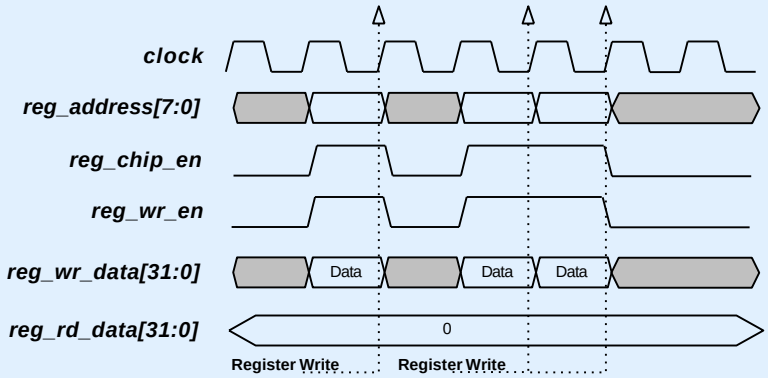
Register Interface

A simple 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application (e.g. I^2C, 8-bit, big-endian, little-endian, etc). The register-core can be interface directly with the Altera SOPC builder via the Avalon bus using a zero wait-state configuration.

Register read access:



Register write access:



Altera® Megacore®

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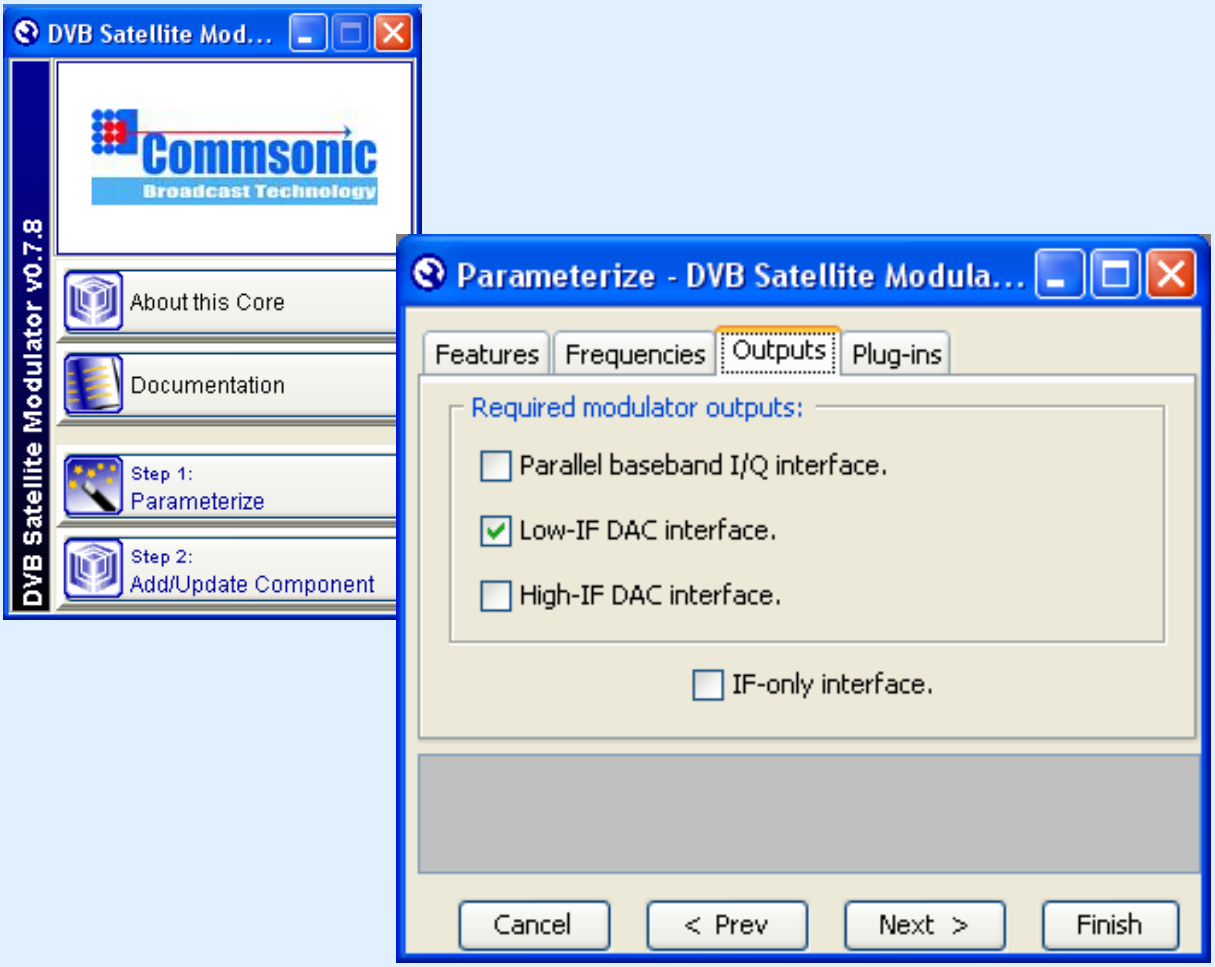
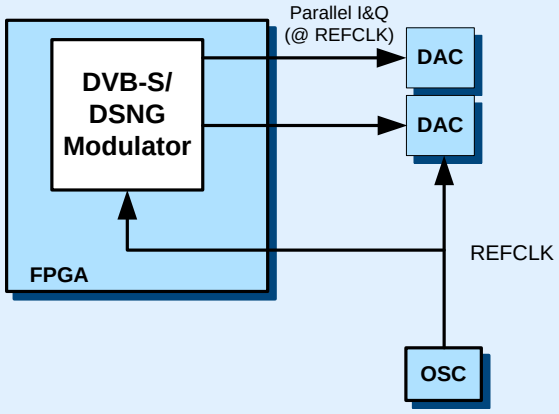
The DVB-S/-DSNG Modulator core provides a number of parameters that can be modified to provide an optimal solution for the targeted technology and/or application. These parameters are available for synthesis time modification using the Megawizard tool within the Altera® Quartus®II software.



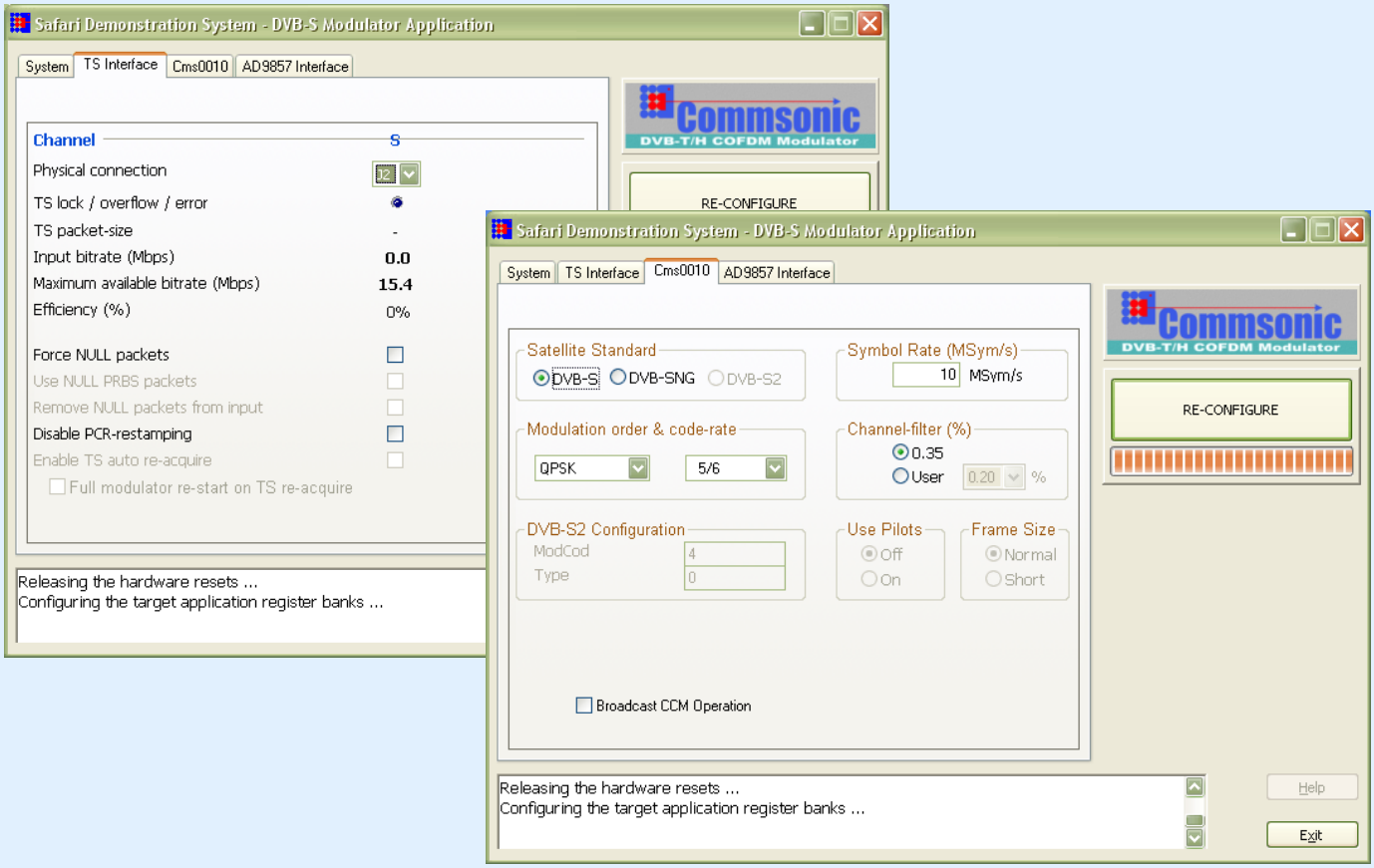
EXAMPLE APPLICATIONS

Up-sampled output using internal interpolation & up-conversion:

This application uses the DVB-S/-DSNG modulator core with internal interpolation that allows the symbol-rate to be changed via a simple s/w register change. The DVB-S/-DSNG modulator internal up-conversion is also used which allows direct connection to external DAC devices



EVALUATION



About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, ATSC-8VSB, ISDB-T, DVB-C/J.83/A/B/C, DVB-T/H and DVB-T2.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.

Commsonic Ltd.
St. Johns Innovation Centre
Cowley Road
Cambridge
CB4 0WS
England

www.commsonic.com
sales@commsonic.com
tel. +44 1223 421845
fax +44 1223 421845